A Signal-Specific Integrating Analog-to-Digital Converter for Biomedical Applications

E. Rahiminejad and R. Lotfi

Abstract: This work describes a modified architecture for integrating analog-to-digital converters (ADC) for use in biomedical or any other applications where the input signal has small and slow variations. In this architecture, instead of digitizing every new analog sample independently, the difference of the new sample with the previous sample is converted to digital. With this idea, the power consumption of the integrating ADC can be considerably reduced. In this paper, design considerations and simulation results of an 8-bit, 4 kS/s ADC in a 0.18μm CMOS technology are addressed to show the effectiveness of the idea. The proposed ADC is more power efficient when used for input signals that are very slow and have small variations in voltage amplitude. Simulations confirm that the proposed ADC architecture shows more than 80% power saving compared to conventional architectures for an input signal amplitude of 0.2 V_{FS}.

Keywords: Low-power, integrating ADC, biomedical applications, signal-specific.

1. Introduction

Integrating analog-to-digital converters (ADCs) are commonly used for high-accuracy yet low-speed applications [1-3]. These converters have very small offset and gain errors and are highly linear. Another advantage of integrating A/D converters is the small amount of circuitry required in their implementation that makes them suitable for ultra-low-power applications. Biomedical signals are often very slow (<1 kHz) and have limited dynamic range. But, power consumption and area are important considerations for these applications.

Also, for many biomedical signals, the difference between two successive samples is much smaller than the full-scale voltage. Therefore, digitizing the difference signal instead of each new sample independently, can lead to considerable power saving [4-7]. In this paper, a novel architecture for an integrating ADC on this idea is proposed. In this architecture, if the input signal changes

very slowly, that is the case for many biomedical signals, the ADC will operate for a short time proportional to the difference between successive values and will go to power-down mode for the rest of the time where the comparator and the counter are switched off and only the output latches and the digital circuit consumes power.

The rest of the paper is organized as follows: Section 2 introduces the conventional integrating ADCs and explains dual-slope and singe-slope architectures commonly used in these ADCs. Section 3 explains the architecture of the proposed ADC. Circuit design considerations are discussed in Section 4. Simulation results of the ADC and a discussion on the effectiveness of the proposed architecture are addressed in Section 5 followed by conclusions in Section 6.

2. Background

Integrating ADCs are divided into two types of dual-slope and single-slope ADCs. In this section, these two types of ADCs are briefly explained.

A. Single-Slope ADC

A simple structure for an integrating ADC, reported in [2], is an implementation example for a single-slope ADC shown in Fig. 1. In this structure a current reference, I_0 is used instead of a voltage reference. Therefore the slope of discharging the capacitor is proportional to I_0.

The circuit works as follows. During Φ1, S1 and S3 are closed, and the input voltage, V_{in}, is stored in C_{int}. During Φ2, S4 and S5 are closed to shift the voltage of C_{int} by V_{ref}. During Φ3, S2, S4, and S5 are closed to discharge C_{int} by the constant current of I_0; meanwhile, the counter measures the time for C_{int} to be discharged back to V_{ref} [2]. Therefore, the digital value stored in the counter, is the digital counterpart of the input analog sample.

B. Dual Slope ADC

The conventional structure mostly used in the high resolution ADCs, is the dual-slope ADC with less sensitivity to the offset voltage of the operational amplifier (OpAmp) compared to the single-slope ADC. This architecture has less dependency on the time constant of the integrator, as well. A simplified diagram for a dual-slope integrating converter is shown in Fig 2 [1].
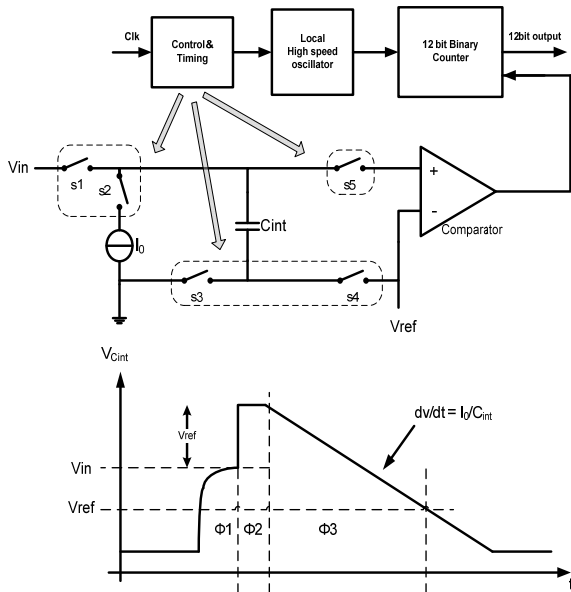
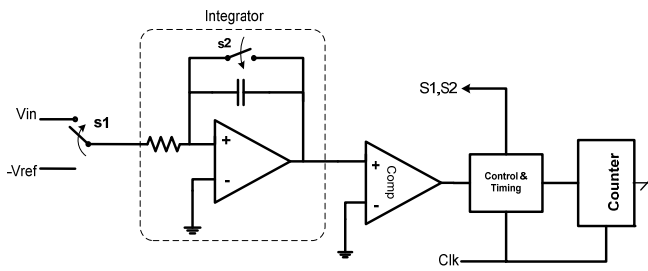Fig. 1. Block diagram and timing diagram for another integrating ADC [2].

Fig. 2. Implementation of Dual-slope ADC [1].

3. The Proposed Low-Power A/D Conversion

Conventionally, in both types of integrating ADCs, each new sample is considered independently regardless of the value of the previous sample. This fact reduces the power efficiency of the ADC. Also, after the comparison, the comparator is not required until the next sampling period. Thus we can turn off the comparator during this time. Here, we propose a modified implementation for a single-slope integrating ADC based on digitizing the difference between two successive samples, instead of digitizing each sample independently.

In many applications, most of the time, the difference between the values of two successive samples of the analog signal is small compared to the signal full-scale range. From power-consumption viewpoint, it thus seems advantageous to digitize the difference of the new sample with the previous sample instead of digitizing every new sample independently. Specifically, in an image sensor, the difference between the intensity of light (and thus the corresponding voltage of the pixel) between two adjacent pixels is much smaller than the full-scale range. In time domain, also, the difference of the light intensity of two successive frames is usually much smaller than the full-scale range. Therefore, if an individual ADC in addition to a multiplexer are used in the image sensor, digitizing the

differences of the pixels' voltages instead of each pixel seems reasonable.

In the integrating ADC, the power is mainly consumed in the counter, the operational amplifier of the integrator and the comparator. Therefore, if these blocks are functioning just for digitizing the differences of successive samples which takes much less time than each new sample independently, and are turned off during the rest of the time, considerable power will be saved [4].

Therefore, instead of conventional A/D conversion, we can store the output of each conversion and only measure the difference between each new sample with the stored value. Hence, the counting time of the counter in every conversion is reduced and the counter as well as the comparator can be turned off until the next sample is being sampled (in a synchronous sampling). This idea can save a great amount of power in applications in which the input voltage changes are not very fast and large.

Fig. 3 compares the timing diagrams of the conventional and the proposed integrating ADCs. As can be observed for the given example, the circuit in the proposed architecture is idle for most of the time and thus the power consumption is much lower; nevertheless, the power consumption is proportional to signal activity [4].
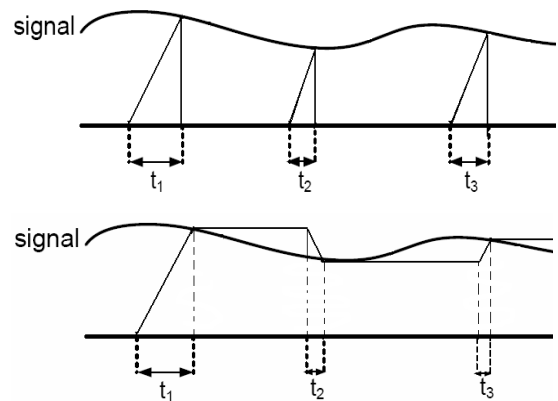

Fig. 3. Comparison of timing diagrams for the conventional and the proposed architecture a) Conventional Integrating ADC b) Proposed Integrating ADC [4].

For implementing the idea, the architecture reported in [2] has been modified as shown in Fig. 4. A current source is used to charge (or discharge) the integrating capacitor, C_{int}, to the value of the input sample. For each new sample, if the value of the sample, V_{new}, is higher than the value of the previous sample, V_{old}, S0 is connected. Hence, I_{ref} charges the capacitor and the counter counts up until it is stopped by the comparator. If V_{new} is lower than V_{old}, S1 and S2 are connected and the mirrored current of I_{ref} discharges the capacitor. In this case, the counter counts down until the comparator stops it at the new value. As soon as the comparator stops the counter, both the counter and the comparator will go to the power-down mode thus considerable power is saved.
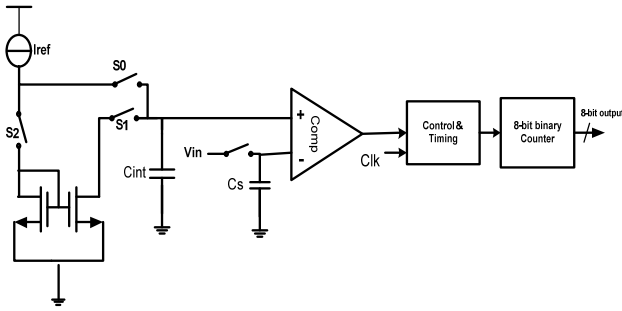
Fig. 4. The block diagram for the proposed architecture.

4. Implementation of the ADC

In this section, practical implementation considerations of an ADC with the proposed architecture are addressed. The proposed ADC includes a reference current, I_{ref}, the comparator and the counter. The maximum time required between two consecutive samples, T_{max}, equals

$$T_{max} = T_s = \frac{1}{f_s} = \frac{C_{INT} \times V_{FS}}{I_{ref}} = 2^N T_{clk} \tag{1}$$

Where T_s and f_s are the sampling period and frequency, respectively and N is the resolution of the ADC. Hence we can specify the value of C_{int} and I_{ref} according to (1). Here, required specifications for the current source and the comparator are first discussed and then the sources of error and dual-supply method for power saving of digital circuits are investigated.

A. Current Source

For a non-ideal current source where the output impedance is finite, the value of the current will be dependent on the output voltage therefore introducing a non-linearity to the entire ADC. In order to reduce this non-linearity below the accepted level imposed by the ADC resolution, the output impedance must be high enough. The current source proposed in [8] has been employed in this work.

B. Comparato

The most important part of this ADC is its comparator because, not only the comparator resolution must be smaller than the ADC resolution, but also a reasonable speed is required to have a minimum delay in the comparator. Note that D_{out} is proportional to the time measured by the counter beginning from the sampling instance until the comparator output changes. Therefore the delay of the comparator influences on the measured time.

Another consideration in the comparator design is the fact that the input common-mode voltage of the comparator varies for different levels of the input sample. In order for the comparator to be fully functional with acceptable performance for the entire input common-mode range, the architecture proposed in [9] has been modified to the circuit configuration depicted in Fig. 5.

C. Error Sources

The most important design concern in the proposed architecture is the accumulation of errors from one sample to another. Four main error sources in this ADC are considered that are the finite output resistance of the current source, the time error of the counter, the comparator offset and the quantization error.

For these error sources, regarding the value of V_{LSB}, the circuits should be designed in a way that the entire error due to the error sources can be ignored compared to V_{LSB}. For the current source, one can write:
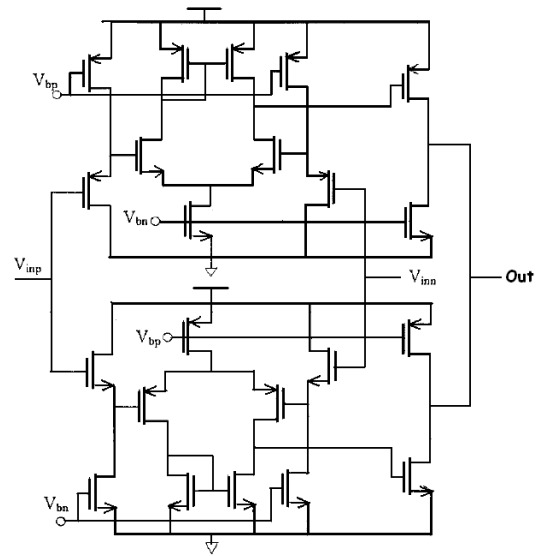

Fig. 5. Rail to rail comparator.

$$I_{ch\,arge} = I_{ref} + I_{error} = I_{ref} + \frac{V_C}{R_{out}} \tag{2}$$

$$\Delta V_C = \frac{I_{error}}{C_{INT}} \Delta t_e \quad , \quad \Delta V_C = \frac{V_C}{R_{out} \times C_{INT}} \Delta t_e \tag{3}$$

$$\Delta t_e = C_{INT} \left(R_{out} \times Ln \left(\frac{R_{out} I_{ref}}{R_{out} I_{ref} - V_{FS}} \right) - \frac{V_{FS}}{I_{ref}} \right) \tag{4}$$

$$\Delta t_e \ll T_{clk} \tag{5}$$

Where Δt_e is the time error of the counter that is calculated with solving the differential equation shown in (2) & (3). By solving the above equation, the minimum value of R_{out} can be calculated.

The time delay between the instant when the comparator sends the stop signal and the end of the counter clock period is corresponding to an error, the second source of error in integrating ADCs. In order to insure that these timing errors are not accumulated, one can simply reset the ADC every *M* samples.

The third error is the offset voltage of the comparator. Here, we show that this offset voltage affects the accuracy of the AC just for the very first sample after resetting the ADC. Assuming an offset voltage of V_{OS} for the comparator (and no other error sources in the ADC), at the beginning of second cycle, the integrating capacitor voltage would be equal to $V_{in0} - V_{OS}$ and the measured time equals

$$\Delta t_0 = C_{int} \frac{(V_{in0} - V_{os})}{I_{ref}} \tag{6}$$

Now, for the following sample, the capacitor will be charged to $V_{in1} - V_{in0}$, since

$$\Delta t_1 = C_{int} \frac{(V_{in1} - V_{os} - (V_{in0} - V_{os}))}{I_{ref}} = C_{int} \frac{(V_{in1} - V_{in0})}{I_{ref}} \tag{7}$$

and similarly

$$\Delta t_N = C_{int} \frac{(V_{inN} - V_{in(N-1)})}{I_{ref}} \tag{8}$$

Therefore, we can eliminate this amount of offset by adding a calibration phase when the ADC starts. But when the offset voltage is not constant we have to add an offset cancelling phase to eliminate the offset of the comparator.

Other method that we used to decrease the amount of accumulated error in the counter is applying an error correction circuit in the digital part of the ADC. The output of the ADC is the digital output of the counter that measures the time where C_{INT} is charging or discharging. One of the main accumulative errors in this ADC is the difference between the analog time of charging the integrating capacitor and the digital counted time of the output. This error is not important in conventional integrating ADCs. But in the proposed ADC, because of the accumulation of errors, it can make a large error in the digital output.

Fig. 6 illustrates the suggested circuit for decreasing this error. The circuit includes two D-flip-flops to convert the analog intervals to an integer counted time for the counter.

As shown in Fig 7, when the input signal (up for charging or down for discharging) changes, this change influences the output only when the clock is on the falling edge. Therefore, in the output we will always have an interval that can be counted with integer number of clocks. Using this method, the accumulative error in the digital output of the counter, has been effectively eliminated.
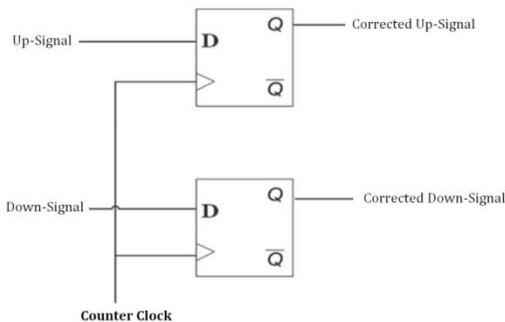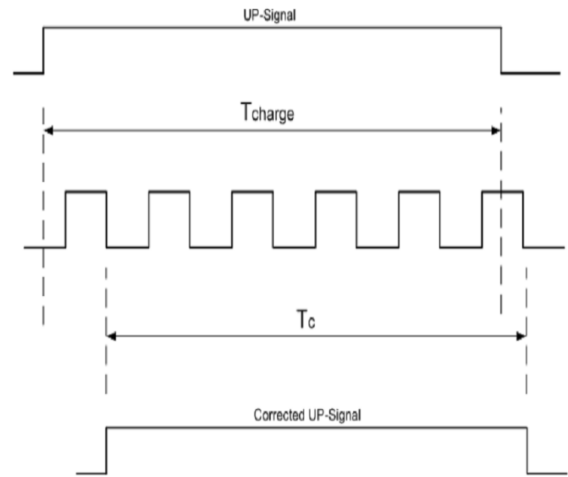

Fig. 6. Error correction circuit.

Fig. 7. Timing diagram of the error correction circuit.

A. Power Saving With Dual-Supply Method

In a conventional integrating ADC, the logic of this type of ADCs is independent from the analog part. Thus we can use a lower voltage supply for the digital part of the ADC. This is because of two important properties of integrating ADCs: firstly, due to the low speed of the ADC, the speed of the ADC is not limited by the digital part. Therefore we can choose lower voltage source for digital part to reduce the power consumption of the logic and the counter circuits. Secondly, since the outputs of the digital circuit are not returned to the analog part of the ADC, there is no need to additional circuits called level converters.

Fig. 8 shows the diagram of the contributions of different parts in the power consumption of the proposed integrating ADC for two values of the supply voltage of the digital part. Simulations show that the power dissipation of the digital part of the ADC contributes 25% of the total power consumption of the ADC for VDD=1.8V. But when we decrease the digital voltage source to 0.5V, the power dissipation of the digital part will be only 4% of total power consumption of the ADC.
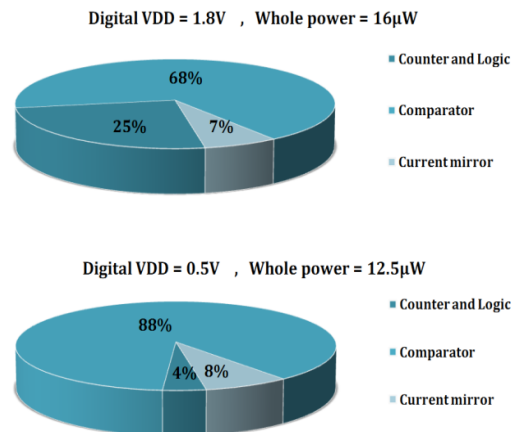

Fig. 8. Pie diagram of power dissipation of different parts of ADC for VDD=0.5V,1.8V.

As a result we can see a 22% reduction in the total power consumption of the ADC.

5. Simulation Results

We designed an 8-bit 4kS/s ADC with a full-scale voltage (V_{FS}) of 1V in a 0.18μm CMOS process. The ADC has been simulated using HSPICE. In this implementation, with a reference current of 0.1μA, the integrating capacitor has been chosen equal to 25pF. Simulation results show that the amount of accumulated error is less that 1 LSB in every 40 samples. So we can reset the ADC in every 32 input samples to assure that the accumulated error is less than 1 LSB.

Fig. 9 shows the 64-point FFT plot of the ADC with the input frequency of $(15/64)*f_S$. The total power dissipation is 16 μW with $0.8V_{FS}$ input amplitude. The value of signal-to-noise-and-distortion ratio (SNDR) is 40dB. The specifications of the ADC are summarized in Table 1.

Table 2 shows the power dissipation for the conventional single-slope ADC and the proposed architecture for different values of the frequency and the amplitude of the input sine wave. It can be observed that a significant reduction in power dissipation is achieved with some complexity overhead in design. For example, for an input signal with an amplitude of $0.2V_{FS}$, at least 80% power saving is observed in the proposed architecture compared to the conventional architecture.

For illustrating the power saving of the presented architecture for low-frequency input signals, we simulated both the proposed and the conventional architectures with an Electrocardiogram (ECG) input signal. Fig 10 shows the digitized output for the ECG signal. Simulation results confirm that the power saving of the proposed architecture for such an input is more than 60%. Furthermore, despite the case for conventional implementations, the power consumption is proportional to the amplitude and frequency of the input signal. Table 3 reports the effectiveness of the new architecture for ECG input signal.
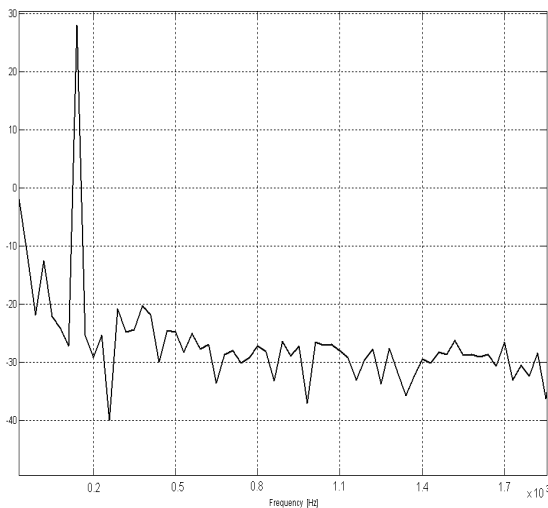

Fig. 9. FFT plot of the ADC– 64 points.

Table 1. Specifications of the ADC.

Technology	VDD	Resolution	Fs	V_{FS}	Power	THD
0.18 μm	1.8	8	4 Ks/S	1V	16 μW	40 dB

Table 2. Power consumption for different frequencies and amplitudes of the input signal.

	0.2 V_{FS}	**0.5 V_{FS}**	**0.8 V_{FS}**
Power Consumption (conventional, f=31/64*fs)	29.2μW	28.8μW	27.6μW
Power Consumption (Proposed, f=31/64*fs)	5.8μW	11.5μW	16μW
Power Consumption (Proposed, f=15/64*fs	4.2μW	7.8μW	11.2μW
Power Consumption (Proposed, f=7/64*fs)	3μW	4.9μW	6.5μW
Power Consumption (Proposed, f=3/64*fs)	1.6 μW	2.7 μW	3.9 μW

Table 3. Power consumption of ADC for ECG input signal.

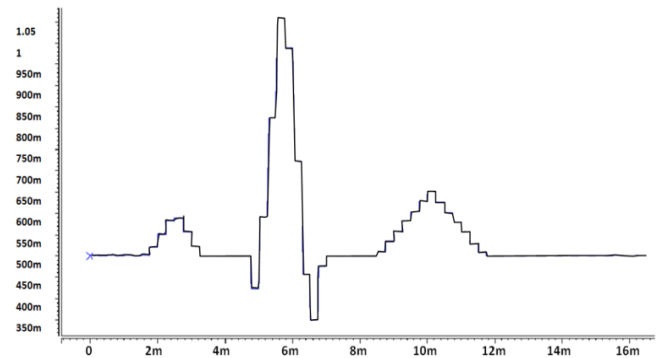| Proposed ADC	12.5 μW
Conventional ADC	31.5 μW

Fig. 10. Digitized output for ECG input signal.

6. Conclusions and Discussions

In this paper, a modified architecture was proposed for integrating A/D converters where the difference between consecutive samples is digitized instead of each new sample independently. Since, most of the ADC parts are turned off during the time in which the ADC is idle, the power saving is considerable for small and slow input signals. HSPICE simulations show that for a $0.2V_{FS}$ input signal, the power of the ADC is reduced from 29.2μW for a conventional implementation to 5.8μWfor the proposed implementation. The power saving is even more for lower frequencies or for biomedical signals such as an ECG signal.

In an image, from one image frame to the other (in the time domain), the difference between the light intensity of two successive images for a specific pixel, compared to the full-scale range, is not very large. Applying the idea explained above in digitizing the differences of samples will therefore considerably reduce the power consumption

of the ADC. Besides, for most of the pixels, the difference between the intensity of light in two adjacent pixels is much smaller than the full-scale range. Thus, if a single ADC as well as a multiplexer is employed, the idea of digitizing the differences of samples seems promising for this case as well.

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Ehsan Rahiminejad was born in Gorgan, Iran, in 1985. He received the B.S. and M.S. degrees in electrical engineering from Ferdowsi University of Mashhad, Mashhad, Iran in 2007 and 2010, respectively. He is currently pursuing the Ph.D. degree in electronics from the Department of Electronics, Ferdowsi University of Mashhad, Mashhad, Iran. He works with the Integrated Systems Lab (ISL), Department of Electrical Engineering, Ferdowsi University of Mashhad. His research interests include the fields of analog-to-digital converters and VLSI circuits. His current research is on a low-power readout circuit for an image sensor in the biomedical applications.

Reza Lotfi received the B.Sc. degree from Ferdowsi University of Mashhad, Iran, the M.Sc. degree from Sharif University of Technology, Tehran, Iran and the Ph.D. degree from University of Tehran, Tehran, Iran, all in electrical engineering, in 1997, 1999 and 2004, respectively. Since 2004, he has been with Ferdowsi University of Mashhad, Mashhad, Iran, where he is currently an Associate Professor. From 2008 to 2009, he was with the Electronics Research Laboratory, Delft University of technology, Delft, the Netherlands as a Postdoctoral Scientific Researcher working on Ultralow-power analog and mixed-signal integrated circuits for biomedical applications. His research interests include low-voltage low-power analog integrated circuit design for biomedical applications as well as high-speed data converters for telecommunication systems. Since 2010, Dr. Lotfi has served as an Associate Editor for the IEEE Transactions on Circuits and Systems.