Optimization of Power and Area in Low-Noise CMOS Bio-Signal Amplifiers

I. Madadi, S. Jafarabadi Ashtiani and N. Masoumi

Abstract: Circuit size and power consumption are the most important parameters in integrated bio-potential signal amplifier with low-noise and low-bandwidth requirements. In this paper, we present an analytical method for optimizing differential amplifiers for constant input-referred noise levels. Power-area optimization is performed over 1mHz to 10kHz for a differential amplifier, designed in a 0.18μm CMOS technology. The designed amplifier consumes 22μA from a 1.8V power supply and the total equivalent input-referred noise over the mentioned bandwidth is equal to 2.4μV_{rms}. The results, validated by SPICE circuit simulations, indicate that the amplifier can be optimized for a specific input-referred RMS noise level.

Keywords: Bio-signal amplifiers, MOSFET, Flicker noise, thermal noise, optimization.

1. Introduction

There is an increasing demand for small, low-power and low-noise bio-potential signal amplifiers [1-2]. The crucial issues in acquisition of bio-potential signals are associated with the characteristics of these signals. Electrocardiogram (ECG), Electroencephalogram (EEG) and Electromyogram (EMG) are the most important types of bio-potential signals. The amplitudes of these signals are from few μV to a few tens of mV and their frequency ranges are from near DC to a few kHz.

In conventional bio-signal amplifiers, receiving bio-potential signals are not very crucial when acquirers are supplied from the main power because there is no limitation for power consumption and size of the system. These bio-signal amplifiers are mainly used in clinical locations and their applications are mainly restricted to clinical purposes.

A number of new applications in receiving bio-signals are introduced recently such as brain-computer interface, self-improvement of stress, controlling the behavior, and implanted integrated circuits (ICs).In order to popularize these new applications, it is required to design low-cost and low-noise integrated analog front-end circuits that can be used in portable battery-operated systems. Amplifiers are the key elements of any low-noise, low-power bio-signal integrated analog front-end. Therefore, developing a systematic design is crucial to achieve the required noise, power, and circuit size.

There are lots of methods to design low-noise, low-power analog amplifiers in CMOS technology. Atrade-off based on current consumption, and inversion coefficient was presented in [3].A design methodology based on optimizing the g_m/I_d factor for designing gain boosted amplifiers was presented in [4].The same methodology was used to design amplifier parameters in [5]. Another g_m/I_d design method has been reported for optimization of transistor sizing and OTA's parameters in [6]. It is discussed in [7] that there is a trade-off between current and area size in the input stage of the bio-potential Analog Front End (AFE) due to the low-frequency characteristics of bio-potential signals and low constant input-referred noise required for the amplifiers. In most of the previously-presented designs, there is a lack of systematic and comprehensive study on the effect of power consumption, circuit area, and biasing conditions on the low-frequency noise of the bio-potential amplifiers. Recently, new design methodologies for bio-potential amplifiers are presented [8].

In this paper, a new procedure for optimization of power-area for a simple differential amplifier is introduced for the first time. Here, it is assumed that the amplifier has a specific, input-referred noise. Then, a comprehensive analysis is presented to simultaneously minimize a power-area optimizing function.

This paper is organized as follows. In Section 2, the optimization of the power-area of differential amplifiers is described, whereas the results from analysis and simulations are presented in Section 3. Finally, the conclusions are drawn in Section 4.

2. Optimization of Area and Power

Different values of area sizes and bias current sof transistors at the input stage of an amplifier result in a specific, input-referred noise [7]. In addition, the need for specific input-referred noise levels results in a wide range of area sizing and bias currents for all transistors in complex amplifiers. Therefore, it is crucial to optimize the power-area of amplifiers for a constant input-referred noise.

Fig. 1 shows the schematic of a differential amplifier used to optimize the power-area.

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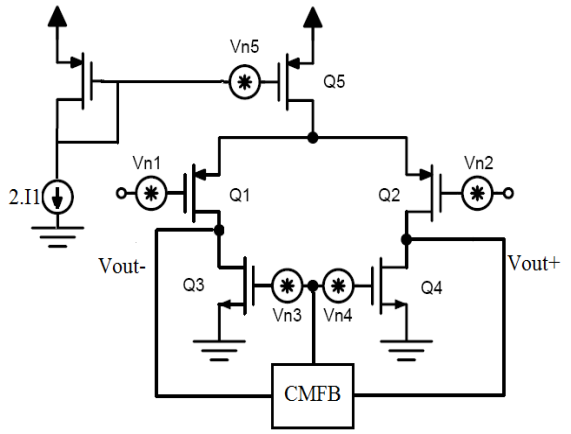

Fig. 1. The differential amplifier used for power-area optimization.

For the fully differential amplifier shown, the total equivalent input-referred RMS noise voltage is given by:

$$S_{in}^2 = 2S_T^2 \tag{1}$$

Where S_T is defined by:

$$S_T^2 = S_{v1}^2 + S_{v3}^2. \tag{2}$$

Here , S_{v1} and S_{v3} are RMS voltage noises of Q_1 and Q_3 at the input of the amplifier. The values of S_{v1} and S_{v3} are composed of flicker and thermal noise voltages. The primary flicker noise voltage is calculated by:

$$V_f = \frac{K(I_d, WL)}{f^{\beta}} \tag{3}$$

Where $\beta$is the constant parameter which is equal to 1 for PMOS transistors and it is near 1 for NMOS transistors.
S_{v1} and S_{v3} are calculated in the AFE bandwidth from the low cut-off frequency (f_L)to the high cut-off frequency (f_H)and are given by:

$$S_{v1}^2 = \frac{k''_{f1}.\left(\frac{I_{d1}}{g_{m1}}\right)^2}{W_1.L_1}.Ln\left(\frac{f_H}{f_L}\right) + \frac{k'_{T1}}{g_{m1}}.(f_H - f_L) \tag{4}$$

And

$$S_{v3}^2 = \left(\frac{k''_{f3}.\left(f_H^{\,1-\beta} - f_L^{\,1-\beta}\right)}{W_3.L_3.(1-\beta)} + \frac{k'_{T3}}{g_{m3}}.(f_H - f_L)\right)\left(g_{m3}/g_{m1}\right)^2 \tag{5}$$

Here, β is a constant parameter and$k''_{f1}$and k''_{f3} are flicker noise coefficients of Q_1 and Q_3, respectively. In both (4) and (5),k'_{T1} and k'_{T3} are constant thermal noise coefficients equal to $\frac{8}{3}K_bT$ where K_b and T are Boltzmann's constant and temperature's value. In both (4) and (5),g_{m1} and g_{m3} are transconductances of Q_1 and Q_3. The parameter g_{m1} is estimated by the EKV model thus it is valid for all of the inversion regions of the MOS transistor [11]. It is given by:

$$g_{m1} = \frac{\frac{2k}{V_t}I_{d1}}{1+\sqrt{1+4IC_1}} \tag{6}$$

Where V_t is the thermal voltage and k is the subthreshold gate coupling coefficient and has a typical value of 0.7 [9].$IC_1$is the inversion coefficient and is equal to I_{d1}/I_{s1} where $I_{s1}$is the moderate inversion characteristic current introduced in [10]:

$$I_{s1} = \frac{2\mu_1 C_{ox} V_t^2}{k}\left(\frac{W_1}{L_1}\right). \tag{7}$$

If IC<0.1, the device operates in weak inversion region and if 0.1<IC<10, the device operates in the moderate inversion region. If IC>10, the device operates in strong inversion region.
In (5), g_{m3} is estimated by the simple above threshold model as

$$g_{m3} = \sqrt{2\mu_3 C_{ox}\frac{W_3}{L_3}I_{d1}}. \tag{8}$$

To find the optimized power and area size for a specific input-referred RMS noise voltage, the relationships between the area of Q_1 and Q_3 and their currents can be obtained from (4) and (5) as:

$$W_1L_1 = {A_1}/{S_{v1}^2} \tag{9}$$

and

$$W_3L_3 = {A_3}/{S_{v3}^2} \tag{10}$$

Where A_1 and A_3 are given by

$$A_1 = \left(H_{1p}(1+X_1)^2 + H_{2p}\frac{L_1^2}{X_1 - 1}\right) \tag{11}$$

and

$$A_3 = \left(H_{1n} + H_{2n}\frac{L_3^2}{X_3}\right)\left(\frac{(1+X_1)^2}{X_3^2}\right). \tag{12}$$

Here,H_{1p}, H_{2p},H_{1n}, and H_{2n} are constant parameters given by:

$$H_{1n} = \frac{k''_{f3}\left(f_H^{\,1-\beta} - f_L^{\,1-\beta}\right)}{k(1-\beta)}, \tag{13}$$

$$H_{2n} = \frac{2k'_{T3}}{k^{1.5}}\frac{(f_H - f_L)V_t}{i_{s3}}, \tag{14}$$

$$H_{1p} = k''_{f1}\left(\frac{V_t}{2k}\right)^2 Ln\left(\frac{f_H}{f_L}\right), \tag{15}$$

and

$$H_{2p} = \frac{4k'_{T1}}{i_{s1}}(f_H - f_L)\left(\frac{V_t}{2k}\right). \quad (16)$$

In (11) and (12), X_1 and X_3 are equal to $\sqrt{1+4IC_1}$and $\sqrt{1+4IC_3}$, respectively, where IC_3 is the inversion coefficient of Q_3. In (14) and (16), i_{s1} and i_{s3} are constant parameters defined by:

$$i_{s1} = \frac{2\mu_1 C_{ox} V_t^2}{k}, \quad (17)$$

and

$$i_{s3} = \frac{2\mu_3 C_{ox} V_t^2}{k}. \quad (18)$$

According to (2), since the total equivalent input-referred RMS noise is comprised of S_{v1}^2andS_{v3}^2, it is important to choose a suitable value for the noise contribution of Q_1 and Q_3.In order to optimize the power versus area for a constant input-referred noise for the whole AFE, it is required to define a power-area product function. By solving the derivation of $Ar_T I_{d1}^{\alpha_2}$as the power-area product function with respect to S_{v1}, where Ar_T is the total area size of Q_1 and Q_3 and α_2 is a constant optimization factor, the proportion of noise contributions is obtained as:

$$S_{v1}^2 = S_T^2.\left(\frac{\sqrt{A_1}}{\sqrt{A_1}+\sqrt{A_3}}\right) \quad (19)$$

and

$$S_{v3}^2 = S_T^2.\left(\frac{\sqrt{A_3}}{\sqrt{A_1}+\sqrt{A_3}}\right). \quad (20)$$

By substituting (19) and (20) in (9) and (10), we can find the total area of the transistors as a function of the equivalent input-referred RMS noise. The total area of amplifier as a function of S_T is equal to

$$Ar_T = \frac{\left(\sqrt{A_1}+\sqrt{A_3}\right)^2}{S_T^2}. \quad (21)$$

It is presented in [7] that $X_1$is a function of L_1 and it is independent from noise. Therefore, A_1 in (21) is constant. The next step is to optimize the area-power product function,$Ar_T I_1^{\alpha_2}$, as a function of X_3. Solving the derivation of the area-power product function with respect to X_3, results in the following equation:

$$L_3^2(F) + L_3(G) + H = 0. \quad (22)$$

Here, *F, G* and *H* are constant parameters given by

$$F = \left(\frac{i_{s1}}{i_{s3}}\right)\left\{\frac{A_1}{L_1^2}\left(\frac{2\alpha_2\gamma}{\alpha_2(1+3\gamma^2)+3(1+\gamma^2)}\right)^2\left(\frac{X_1-1}{X_1+1}\right)\right\}, \quad (23)$$

$$G = -\left(H_{2n}\frac{L_1\sqrt{\frac{i_{s3}}{i_{s1}}}}{\gamma\sqrt{X_1^2-1}}\right), \quad (24)$$

and

$$H = -H_{1n}, \quad (25)$$

where γ^2 is a ratio of W_1L_1 to W_3L_3 given by

$$\gamma^2 = \frac{\frac{L_1^2}{i_{s1}(X_1^2-1)}}{\frac{L_3^2}{i_{s3}(X_3^2-1)}} = \frac{\sqrt{A_1}}{\sqrt{A_3}}. \quad (26)$$

Now, by assuming an arbitrary value for γ, the proper value of L_3 is obtained from (22) and in the next step X_3can be extracted from (26). By substituting L_1, X_1, L_3 and X_3in (19), the value of S_{v1}^2 is obtained. Therefore, the width of the transistor Q_1 is calculated by (9). Eventually , I_{d1} will be calculated in terms of

$$I_1 = \frac{W_1}{L_1}(X_1^2-1)\left(\frac{i_{s1}}{4}\right) \quad (27)$$

or

$$I_1 = \frac{W_3}{L_3}(X_3^2-1)\left(\frac{i_{s3}}{4}\right). \quad (28)$$

In order to solve the derivation of power-area product respect to X_3, some simplifications are used, resulting in an error in calculations. The relative error of calculated γ can be defined as ERR and it is given by

$$ERR(\%) = \frac{\gamma_{cal}-\gamma}{\gamma}.100 \quad (29)$$

Where γ_{cal} is the calculated version of γ after the optimization is done and it is defined as

$$\gamma_{cal} = \sqrt{\frac{W_1L_1}{W_3L_3}}. \quad (30)$$

3. Simulation Results

In this section the results from (1) to (30) are calculated and

analyzed by numerical simulations. Finally, these results are validated by SPICE simulations. This section is divided into two parts. In part *A*, the numerical simulations are shown and results are analyzed. In part *B*, SPICE simulations are illustrated and the results from both parts are compared. All the simulations in this section are performed in a standard 0.18μm CMOS technology.

A. Numerical simulations

In this section, all simulations are performed for a constant total equivalent input-referred RMS noises over 1mHz to 10kHz. Fig. 2 shows the total area of transistors Q_1 and Q_3 in Fig. 2 (a) and the area size of transistor Q_1 in Fig. 2 (b) as a function of total current for 2.6μV_{rms}. The lengths of Q_1 and Q_3 are equal to $4L_{min}$ and $80L_{min}$ where L_{min} is defined as the transistor minimum length of CMOS technology. In this step, W/L of Q_1 and Q_3 are swept and the values which meet the noise requirement are selected. The resulting amplifier circuits with an input RMS value, up to 5% close to 2.6μV_{rms} are selected from more than 100000 simulation points and their associated area-current points are placed in Fig. 2. The discontinuity of the graphs is due to the limited number of simulations. The minimum of the area size can be seen in Fig. 2 (a).The noise performance of the amplifier is dominated by transistor Q_1, located in the input stage of the amplifier. Therefore, it is realized from Fig. 2 (b) that the minimum area size is the result of Q_1 as the input stage. If α_2=0, there will be no value for L_3 to satisfy (22).In other words, the minimum of total area of the amplifier is controlled by Q_1.S_{v1} and S_{v3} versus current are depicted in Fig. 3. S_{V1} is approximately equal to 1.2μV_{rms} in low current values. Furthermore, it is seen that by increasing IC_1, I_d and g_{m1} increase. Therefore, the thermal noise voltage of Q_1 decreases and the flicker noise voltage of Q_1 should be increased since S_{v1} is constant.

According to Fig. 2(b), it can be seen that the area size of Q_1 decreases by increasing the flicker noise contribution of Q_1 and Q_3 is changed because of an abrupt increase and decrease in the values of g_{m2} and g_{m1}, respectively. The area of Q_1 increases at high current values due to an abrupt decrease in the value of S_{v1}.

The values of L_3/L_{min} versus IC_3 for various values of α_2, 2.0μV_{rms} input referred noise, and L_1=$2L_{min}$ is illustrated in Fig. 4. Regions *A* and *B* show the strong and moderate inversion regions. Therefore, it can be seen that Q_1 operates in moderate and strong inversion regions for all values of α_2.

Fig. 5 shows the current consumption and total area size of Q_1 and Q_2 versus γ for various values of α_1, which has been defined in [7] as the optimization factor of the input stage of the amplifier. L_3/L_{min} versus γ is illustrated in Fig. 6. It can be realized that by increasing the value of γ, the optimum value for the length of Q_3 increases, as shown in (22). It is obvious that by increasing α_1, the optimized current is reduced. If the value of α_1 increases the value of optimized current decreases because the value of α_1 determines X_1 and the optimum proportion between area and current. As demonstrated in (22), the value of L_3 changes by X_1. Therefore, according to Fig. 6, a smaller α_1 leads to a smaller L_3. Also an increase in γ results an abrupt increase in the optimized value of L_3. The highlighted parts in Fig. 5 and Fig. 6 show appropriate regions for the value of γ.

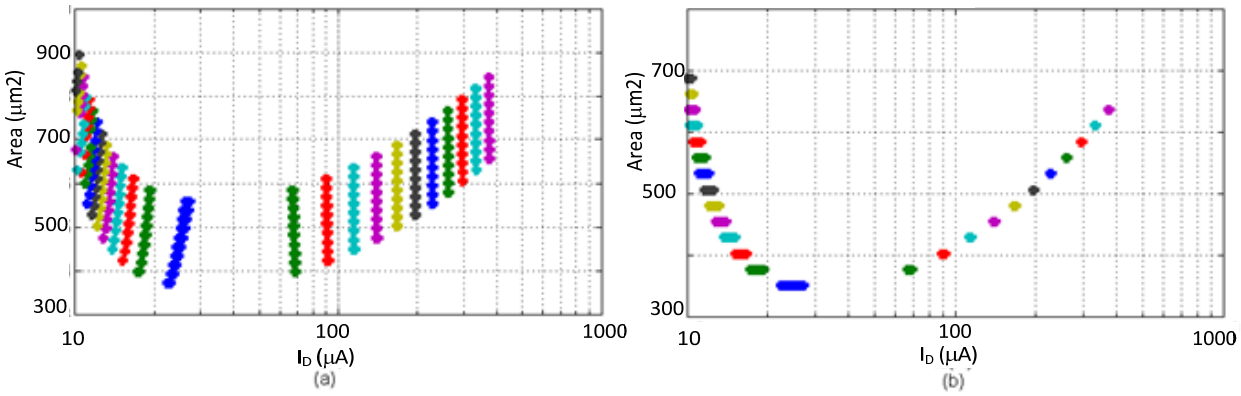

Fig. 2. Area versus current for 2.6µV_{rms} input referred noise. a: total area of Q1 and Q3, b: Area of Q1.

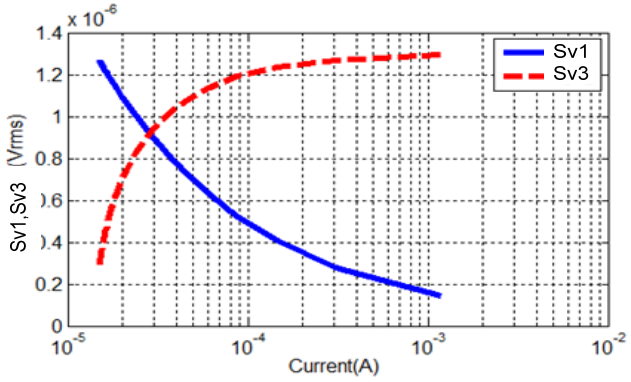

Fig. 3. Noise contribution of transistors Q_1 *and* Q_3 (S_{v1} and S_{v3}) versus current for 2.6μV_{rms} input referred noise.

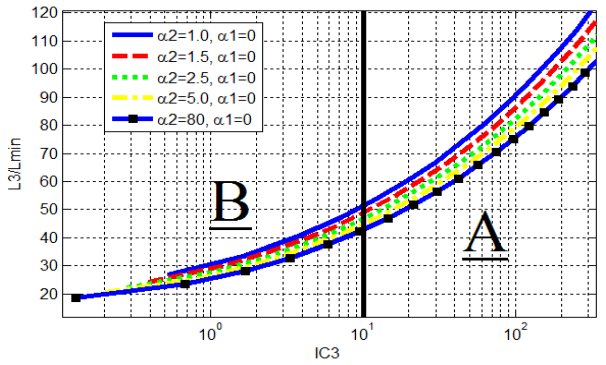

Fig. 4. L_3/L_{min} ratio versus IC_3 for various $\alpha_2$values, 2.0μV_{rms} input
referred noise, and L_1=2.L_{min}.

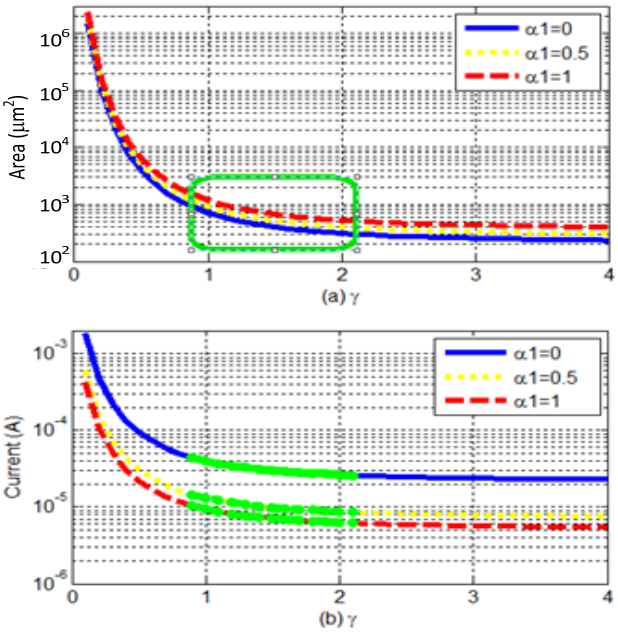

Fig. 5. (a) Total area of Q_1 and Q_3.(b):Current of Q_1 versus γ for various α_1 values α_2=2.5, L_1=2.L_{min} and input referred noise is 2.0μV_{rms}.

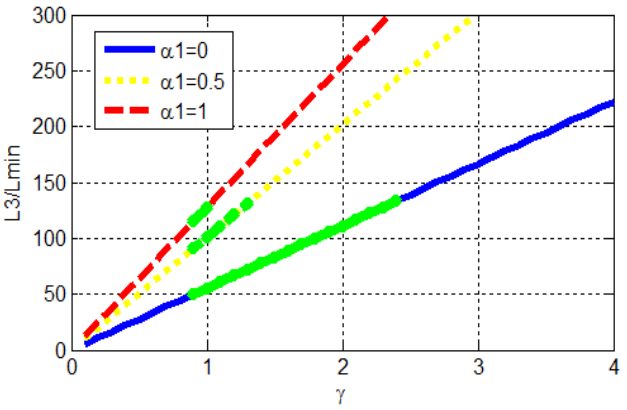

Fig.6. L_3/L_{min} versus γ for various $\alpha_1$values for 2.0μV_{rms} input referred noise.

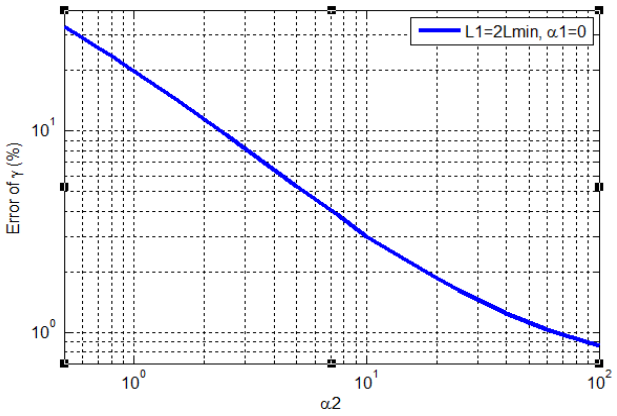

Fig. 7. Error percent of calculated γ versus α_2.

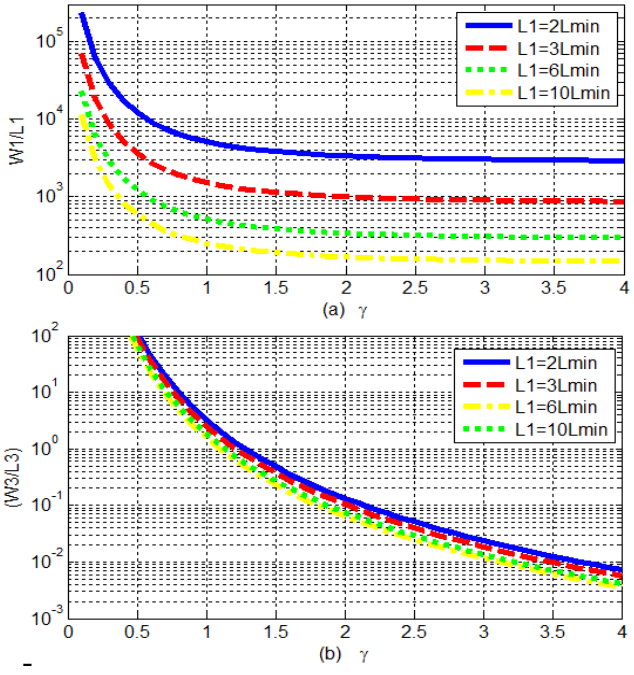

Fig. 8. *W/L* of transistors *Q1* and *Q3* versus γ for $\alpha 2$=2.5,$\alpha 1$=0 and
2.0$\mu Vrms$ input referred noise.

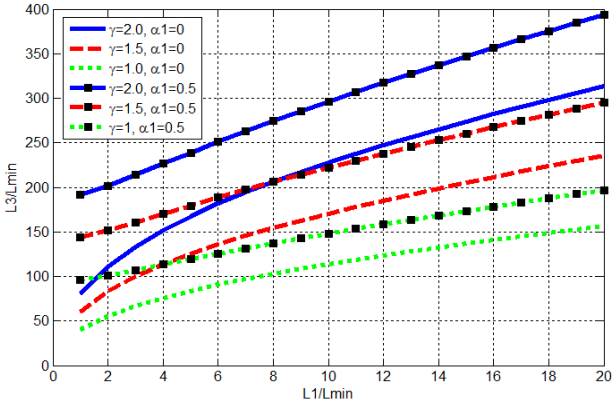

Figure. 9. L_3/L_{min} versus L_1/L_{min} for various α_1 and γvalues for 2.0μV_{rms} input referred noise.

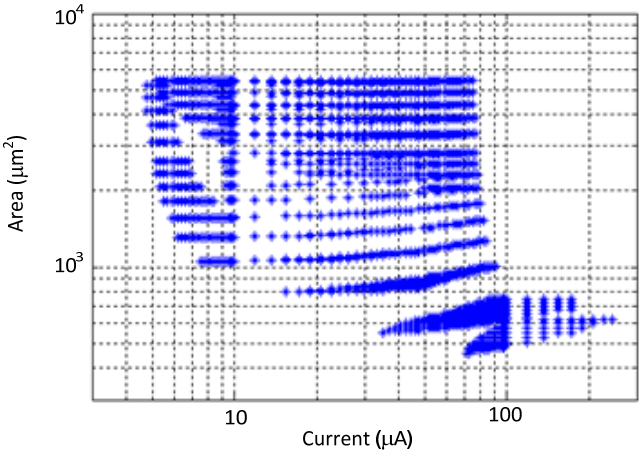

Fig. 10. Total area of the amplifier versus current consumption for 2.0μV rms input referred noise, L_3=60.L_{min} and L_1=4.L_{min}.

The relative error of the calculated γ versus α2 is depicted in Fig. 7. The error becomes higher than 30% for a smaller α2 and if α2 is selected higher than 2.5 then the error becomes smaller than 10%. W/L of Q1 and Q3 versus γis shown in Fig. 8. It is obvious that for all the assumed values of the length of Q1, W/L of Q1 and Q3 are obtained so that Q1 and Q3 operate in weak and strong inversion regions. High W/L values cause the gate-source voltage of Q1 to drop. As a result, the transistor operates in moderate or weak inversion regions. On the contrary, Q2 tends to operate in moderate and strong inversion. Therefore, in order to operate in those regions at a constant current, it is required to increase the gate-source voltage by decreasing W2/L2.

Selecting an appropriate value for L_1 is very important because the proper value of L_2 is directly influenced by L_1, as predicated by(22);thus, the optimized L_3 is a function of L_1. An increase in L_1 results in an increase in L_3. The variations of L_3/L_{min} versus L_1/L_{min} are shown in Fig. 9 for various values of α_1 and γ. In order to get rid of high optimized channel length values for Q_3, it is essential to choose a lower L_1.

B. SPICE simulations

In this part SPICE simulations are invoked to validate the numerical simulations. All the simulations are performed in a standard 0.18μm CMOS technology. Firstly, the parameters α_1, γ and L_1 are assumed to be arbitrary values and L_3 is calculated. Then, the current values and W/L of transistors are swept widely and the RMS voltage of the input-referred noise is calculated. Finally, all the points which meet the noise specification are extracted. Fig. 10 shows the area versus current for L_1=4.L_{min} and L_3=60.L_{min} for an RMS input-referred noise voltage equal to 2μV. The discontinuities in the graph are due to the limited number of simulation points.

It is overtly clear that there is a trade-off between the area versus the current. The trend of the whole circuit is followed by the input stage. The areas of Q_1 and Q_3 rise abruptly to obtain a constant noise performance for small currents.

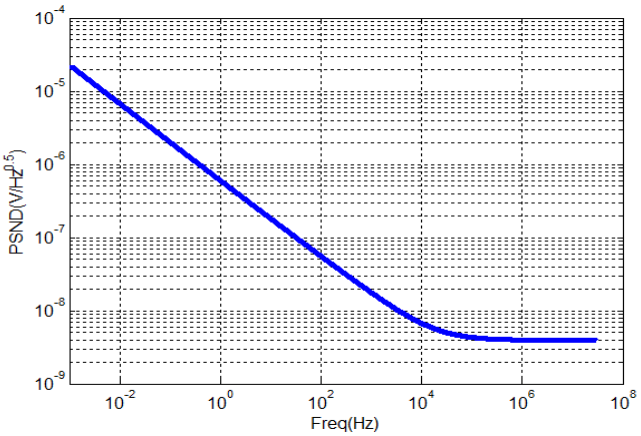

Fig. 11. The power spectral density of the input-referred noise of the amplifier.

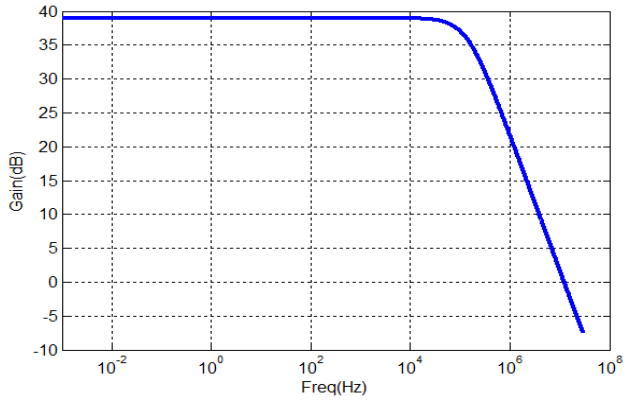

Fig. 12. The frequency response of the amplifier.

By following all the equations from the previous section and assuming that L1=2.Lmin, γ=1.5, α1=0.3 and α2=5 the length value of Q3 is obtained by (22), therefore L3=110.Lmin, W1/L1=4400, W3/L3=0.5 and current value

of Q1 is equal to 22μA. The total area of Q1 and Q3 is equal to 0.8E-9m2. The power spectral density of the input noise of the whole amplifier is illustrated in Fig. 11 and the frequency response of the amplifier is shown in Fig. 12. The unity gain bandwidth of amplifier with load capacitance equal to 5pF is equal to 12.7MHz and the DC gain of amplifier is equal to 39dB. The input-referred noise of amplifier over 1mHz to 10kHz is equal to 2.4μVrms.

4. Conclusion

An analytical method for optimization of a differential amplifier has been presented and the results were compared with those obtained from SPICE simulations. This amplifier was designed in 0.18*μm* CMOS technology and both flicker and thermal noise voltages have been considered in the circuit model and the simulations. The inversion coefficients, current values, width of transistors, and the optimum length value of transistors are obtained for a specific RMS input-referred noise voltage over the frequency range of 1mHz to 10kHz. In order to achieve a high performance for acquisition of bio-potential signals, it is essential to bias the input stage transistor and the load transistor in weak or moderate inversion and strong inversion regions, respectively. Finally, the power spectral noise density and the frequency response of the amplifier were derived and presented.

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