MIRIM: Modified Interleaved Repeater Insertion Methodology to Reduce Delay Uncertainty in Global Interconnections

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Abstract: This paper presents an accurate methodology for the optimum interleaved-repeater positioning in global interconnects. We have compared the analytical delay uncertainty of available repeater insertion techniques and derived analytical expressions for extracting a new optimum value for the relative position ratio of the interleaved interconnects. We have used the simple yet-realistic α-power law for MOS devices in the proposed model in order to increase the accuracy of the methodology. The new positioning method has been proven to minimize the delay uncertainty caused by the coupling capacitance of the switching adjacent lines. The measured uncertainty of the proposed methodology was less than 10% for all beyond 100-nm scaled technology nodes. It is also shown that the proposed strategy offers lower propagation delay sensitivity to variations of a segment length in comparison with commonly used repeater insertion techniques. Accordingly, using the proposed methodology, we achieve a maximum sensitivity reduction of 33% for 65-nm technology, 51% for 45-nm technology and 34% for 32-nm technology node.

Keywords: Repeater insertion, interconnect, delay uncertainty, coupling capacitance, switching pattern, crosstalk, VDSM.

1. Introduction

Interconnect delay has become the major limiter to today's high performance VLSI and nano-systems, considering the continuous scaling of CMOS technology [1]-[6]. This leads to the domination of the interconnect delay in comparison with the gate delay, since the number of global wires is increasing with exhaustive integration and these wires do not scale with the technology scaling [7], [8]. The delay of a long interconnect is influenced by the coupling capacitance between the switching adjacent lines. This effect, so called as crosstalk, exhibits a major impact on delay in on-chip busses [9]. Circuit designers should consider the resulting crosstalk noise especially in current nanometer technologies, since the coupling capacitance is continuously growing compared to the total wire capacitance due to the increment of the wire's aspect ratio [10].

Fig. 1 illustrates the ratio of the coupling capacitance to the total capacitance of interconnects for different technology nodes. As it is clear, coupling capacitance composes more than 75% of total wire capacitance in 32-nm technology. Moreover, Miller factor causes the effective wire capacitance of an interconnect to be variable and switching pattern–dependent, resulting in a noticeable delay uncertainty with technology scaling [11]. Considerable work has been done so far to minimize the interconnect noise, as well as degradation in performance regarding the coupling capacitance. Wire switching, shield insertion, and wire spacing have been previously common in reduction of destructive crosstalk effects on propagation delay [12]-[14].

Among all of the delay minimization strategies, repeater insertion has been well accepted to be efficient for reducing signal transition times in very large scale integration (VLSI) circuits [15]. Extensive research has been conducted in the literature for repeater insertion technique in order to reduce delay and delay uncertainty [16]-[30]. Using uniform repeater insertion, better signal integrity and less propagation delay is achieved. The smart repeater methodology, introduced by Weerasekera et al, consists of a main and an assistant driver and is a way to dynamically alter the drive strength depending on the relative bit pattern [25]. Furthermore, the additional parasitic capacitance of the driver circuit as well as the selector logic, which is used to determine the switching pattern of the adjacent lines, makes the methodology impractical in the nanometer regime. Hybrid polarity repeater insertion, introduced in [26] by Akl and Bayoumi, is an effective method to come up with worst-case propagation delay with little sensitivity to repeater placement variation. The proposed technique however exhibits considerable measured uncertainty in SPICE simulations due to the simplified delay equations.
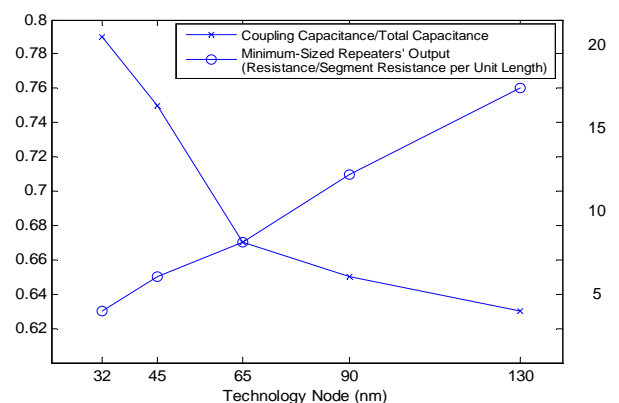

Fig. 1. Ratio of coupling capacitance to total capacitance of an interconnect for different technology nodes based on ITRS 2008.

Position of the repeaters is usually interleaved to further reduce the effect of the crosstalk on propagation delay. Previously, designers have interleaved repeaters exactly midway between the positions of the two repeaters in the bus line. However, an optimum place for interleaved repeater-inserted lines has been introduced in [22] by Ghoneima and Ismail to balance the variable pattern-dependent delay of the adjacent interconnects. The model is a function of the ratio of the output resistance of the repeaters to the segment length resistance of the bus. Since the wire resistance is considerably comparable to the repeater's output resistance in current nanometer technologies (shown in Fig. 1), it has been found that the optimal relative position ratio is around 70% of the total segment length. However, the method described in [22] is highly sensitive to the segment length and repeater placement variations caused by the layout limitations. Thus, it is well accepted that the current repeater insertion methods cannot reduce the delay uncertainty of on-chip busses caused by the destructive switching pattern of the adjacent lines.

In this paper, for achieving the minimum delay uncertainty and segment length sensitivity, a new methodology for interleaved repeater-inserted busses is proposed. Using the idea of interleaved repeater insertion, we have developed a strategy to effectively reduce the worst-case propagation delay of switching interconnects. The α-power law is used to increase the accuracy of the proposed methodology [31]. We have derived an expression for the propagation delay of the interleaved repeater-inserted line considering the static and dynamic capacitive elements. The segment length variation has the least possible effect on the delay fluctuation among the available repeater insertion techniques. Thus, the modified interleaved repeater insertion technique is not sensitive to repeater placement variations resulting from the layout constraints.

The paper is organized as follows. Section II provides an analysis of the existing delay uncertainty reduction strategies. Section III introduces the Modified Interleaved Repeater Insertion Methodology, named as MIRIM, in addition to relative sensitivity derivations. Section IV addresses the simulation results and discussions. Finally, Section V presents the conclusion.

2. Repeater-based Delay Uncertainty Reduction Strategies

In this section, we shall analytically review the delay uncertainty reduction techniques on the basis of repeater insertion which have been previously addressed in the literature. Three repeater insertion methodologies will be analyzed and the analytical delay uncertainties will be compared prior to the introduction of our proposed model. These three strategies are called standard, hybrid, and interleaved repeater insertions. The repeater in this paper is assumed to be implemented as a CMOS inverter, in order to employ delay balancing to overcome the crosstalk induced delay.
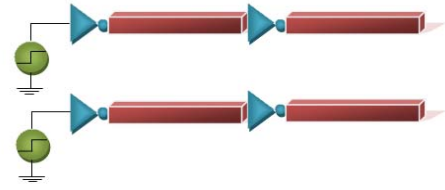

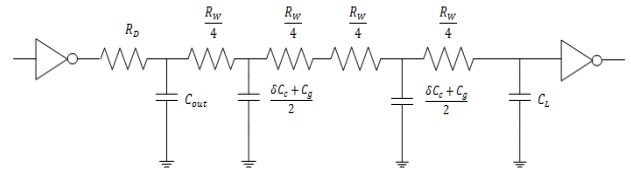Fig. 2. Standard repeater insertion technique.

Fig. 3. Circuit-level modeling of standard repeater insertion technique used for analytical examination.

A. Standard Line

Fig. 2 shows the standard repeater insertion methodology with inverters inserted at the appropriate positions of bus wires. Moreover, the circuit-level modeling of the standard line is illustrated in Fig. 3, where δ is defined as the switching factor between two adjacent lines of a bus. The resistive-capacitive T model is used for each wire sub-segment. Using the Elmore delay model [32], one can write an equation for any repeater-inserted line in order to calculate the delay uncertainty of the transmitted signal. The delay per segment of the illustrated standard line can be written as

$$D_{Standard} = R_D C_{out} + \left(\frac{C_g}{2} + \delta \frac{C_c}{2} \right) \cdot \left(R_D + \frac{R_W}{4} \right)$$
$$+ \left(\frac{C_g}{2} + \delta \frac{C_c}{2} \right) \cdot \left(R_D + \frac{3R_W}{4} \right) + C_L \left(R_D + R_W \right) \quad (1)$$

where, C_g is the line's vertical capacitance component per unit length and C_c is the line's lateral capacitance component per unit length. C_L and C_{out} are the repeater's input and output capacitances, respectively. R_W is the segment's resistance, R_D is the repeater's output resistance, and δ is the switching factor. The delay in (1) is a function of δ, which means that the delay is dynamic and depends on switching pattern. Considering the minimum and maximum values for the coupling coefficient of two adjacent lines as δ_max=0 and δ_min=2, we can calculate the delay variation of standard line segment as

$$\Delta D_{Standard} = 2C_c R_D + C_c R_W. \quad (2)$$

The delay equations mentioned in (1) and (2) are functions of the segment length which is usually assumed to be equal to the optimal value (l_{opt}) for the minimum propagation delay. However, a number of limitations may lead to the repeater insertion to be confined to the borders of the sub-circuit layouts, resulting in a considerable fluctuation in the number of repeaters, their positions as

well as the segment length [33]. Therefore, the sensitivity analysis of the propagation delay of the line to the segment length is significant in any repeater insertion methodology. The sensitivity of the delay of any interconnect segment to its length is defined as [22]

$$S_t(l) = \frac{\partial t_D(l)}{\partial l}. \tag{3}$$

For the standard line, the worst-case sensitivity is expressed as

$$S_{t-Standard}(l) = S_{t0} + 2S_{tc} \tag{4}$$

where S_{t0} and S_{tc} are the static and dynamic sensitivity functions, respectively. S_{t0} is independent of the switching factor (δ), whereas S_{tc} depends on the switching factor and varies while switching. As it is clear, the worst-case dynamic sensitivity function of the standard repeater inserted segment appears in (4) with a factor of 2 which is significant.
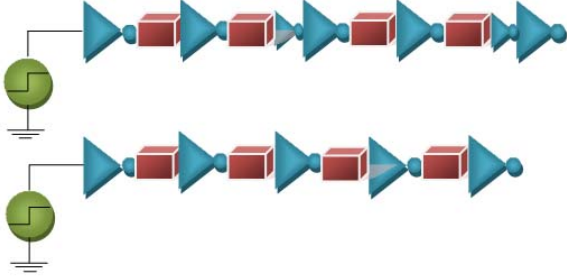

Fig. 4. Hybrid polarity repeater insertion technique.

B.　Hybrid Line

The hybrid polarity repeater insertion methodology is illustrated in Fig. 4. The inverting repeaters at the midpoint of alternate line are replaced with non-inverting repeaters (a pair of sequential inverters) to achieve a constant average capacitive coupling for any possible input transition [26]. Considering the delay balancing in this technique and assuming that the number of segments is even as well as the extra delay of the midway non-inverting is negligible in comparison with the total interconnect latency, the delay fluctuation of the hybrid polarity repeater insertion is half of the standard line segment and can be written as

$$\Delta D_{Hybrid} = C_c R_D + C_c \frac{R_W}{2}. \tag{5}$$

Thus, it is clear that the hybrid polarity repeater insertion cannot minimize the delay uncertainty resulted from the capacitive crosstalk of the different switching lines. Due to the delay balancing methodology addressed in the hybrid repeater insertion strategy, the dynamic delay sensitivity to the segment length is half of the standard line. This leads to the sensitivity expression for the hybrid polarity repeater inserted segment as follows
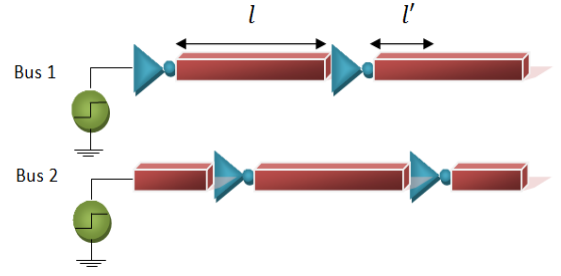
$$S_{t-Hybrid}(l) = S_{t0} + S_{tc}. \tag{6}$$

Fig. 5. Interleaved repeater insertion technique.

C.　Interleaved Line

Fig. 5 illustrates the interleaved repeater insertion technique. This strategy reduces the delay uncertainty due to the fact that when a part of the aggressor line switches in a certain direction, the other part switches in the opposite direction, resulting in the reduction of the net coupling capacitance. The optimum position for the interleaved line is supposed to be $l' = \beta l$ [22] (not necessarily at the midpoint of the segment). The circuit-level modeling of the interleaved line is illustrated in Fig. 6, where β is the ratio of the length of the optimum placed interleaved line to the total line segment, and δ_1, δ_2 are the switching factors of the two sub-segments in the interleaved bus. The resistive-capacitive T model circuits are used for each sub-segment to be helpful in analytical analysis. Three possible values for the switching factors δ_1, δ_2 in the two bus lines illustrated in Fig. 5 are summarized in Table 1.

Table 1. Switching factors for different bus switching patterns

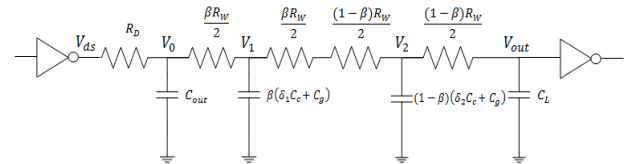| Switching Pattern	δ_1	δ_2
Busses 1 and 2 are switched in the same direction	2	0
Busses 1 and 2 are switched in the opposite directions	0	2
Busses 1 and 2 are inert	1	1

Fig. 6. Circuit-level modeling of interleaved repeater insertion technique used for analytical analysis.

Using the Elmore delay model, we can write an expression for the delay of the interleaved segment as below

$$D_{Interleaved} = R_D C_{out} + (C_g + \delta_1 C_c)\beta.\left(R_D + \frac{R_W}{2}\beta\right) + \\ (C_g + \delta_2 C_c)(1 - \beta).\left(R_D + \frac{R_W}{2}(1 + \beta)\right) + C_L.(R_D + R_W). \tag{7}$$

The switching dependent parts of (7) can be separated to introduce the dynamic delay of the interleaved line as

$$D_{\text{Interleaved}}^{\text{Dynamic}} = \delta_1 C_c \beta \left(R_D + \frac{R_W}{2}\beta \right)$$
$$+ \delta_2 C_c (1-\beta) \left(R_D + \frac{R_W}{2}(1+\beta) \right). \qquad (8)$$

Considering the switching factors mentioned in Table I, we can calculate the delay variation of the interleaved segment by subtraction of the best case delay from the worst case delay as

$$\Delta D_{Interleaved} = 2C_c(1 - 2\beta)R_D + C_c(1 - 2\beta^2)R_W. \qquad (9)$$

It is mentioned in [22] that the ratio of the interleaved repeater-inserted segment to the total line segment, β, is a value between 0.5 and 0.7; therefore, the delay variation of the interleaved segment is bounded as

$$2C_c(\sqrt{2} - 1)R_D < \Delta D_{\text{Interleaved}} < \frac{C_c R_W}{2}. \qquad (10)$$

By equating the equation (9) to zero, we can calculate the optimum value for the ratio of the interleaved repeater-inserted segment to the total line segment as

$$\beta_{\text{opt-Interleaved}} = \frac{\sqrt{R_D^2 + \frac{1}{2}R_W^2 + R_D R_W} - R_D}{R_W}. \qquad (11)$$

The optimum value for β in (11) has been previously introduced in [22] as a function of η, which is the ratio of the output resistance of the repeaters (R_D) to the segment length resistance of the line (R_W). The delay sensitivity of the optimized interleaved repeater-inserted segment to its length can be written as [22]

$$S_t(\beta_{\text{opt}}, l) = S_{t0} + (1 + \sqrt{2}\eta)S_{tc}. \qquad (12)$$

Therefore, it is obvious in (12), that the interleaved repeater-inserted line is highly sensitive to segment length variation, since η is a positive value. Even though the repeater-to-wire segment resistance ratio, η, decreases with continuous technology scaling, circuit designers usually select the optimum values for the segment length as well as the repeater size to minimize the propagation delay prior to using the optimum place for the interleaved line. We have derived expressions for the optimum segment length (l_{opt}) and the optimum repeater size of the interleaved line (k_{opt}) [18], [19] as

$$l_{\text{opt}} = \sqrt{\frac{2R_{D0}(C_{out0} + C_{L0})}{r_W(C_g + 2C_c)}}. \qquad (13)$$

$$k_{\text{opt}} = \sqrt{\frac{R_{D0}(C_g + 2C_c)}{r_W C_{L0}}}. \qquad (14)$$

where C_{L0} and C_{out0} are the minimum-sized repeater's input and output capacitances, respectively. Also, r_W is the segment's resistance per unit length and R_{D0} is the minimum-sized repeater's output resistance. By utilizing equations (13) and (14), we can write the optimum ratio of

the output resistance of the repeaters to the segment length resistance of the line as

$$\eta_{\text{opt}} = \frac{R_D}{R_W} = \frac{R_{D0}}{r_W \cdot l_{\text{opt}} \cdot k_{\text{opt}}} = \frac{1}{\sqrt{2(1 + \frac{c_{out0}}{c_{L0}})}}. \qquad (15)$$

Thus, the optimum value for η is a function of the minimum-sized repeater's input and output capacitances. In current sub 100-nm technologies, $c_{out0} \cong c_{L0}$. Therefore, the optimum value for η is 0.5, which is the minimum possible value as well.

3. Proposed Delay Uncertainty Reduction Methodology

In this section, we shall introduce our proposed technique, which is based on the classical interleaved repeater insertion methodology, to reduce the destructive delay uncertainty due to the coupling capacitance of the adjacent lines. We will use the α-power law for transistors to increase the accuracy of our proposed new methodology.

A. Dynamic Propagation Delay Derivation

The α-power law model describes the short-channel transistor behavior such as the velocity saturation and provides an accurate form of the *I-V* characteristics [31]. Regarding a large portion of the circuit operation (repeaters) occurs in the linear region of CMOS technology, we will use the linear region form of this model to characterize the *I-V* behavior of the ON transistors. We will also consider only the rising input waveform. Our methodology, however, can be applied to the falling input waveform as well. Considering the circuit-level modeling of the interleaved repeater-inserted segment in Fig. 6, we first ignore the input and output capacitances of the repeaters in order to derive an expression for the dynamic propagation delay. As we mentioned before, this dynamic delay is due to the wire capacitance which is a function of the switching factor of the adjacent lines. According to the α-power law model, the N-channel drain current in the linear region ($for\ V_{gs} \geq V_T, V_{gs} - V_T \geq V_{ds}$) is given by [31] as follows

$$i_d = \frac{I_{d0}}{V_{d0}} \left(\frac{V_{gs} - V_T}{V_{DD} - V_T} \right)^\alpha V_{ds}. \qquad (16)$$

Here, V_{DD} is the supply voltage and V_T is the NMOS threshold voltage. I_{d0} is the drive current of the MOS device which is proportional to W/L, V_{d0} is a process dependent constant and is the voltage of drain-to-source (V_{ds}) where the velocity saturation occurs with $V_{GS} = V_{DD}$. Also, α is the process dependent degree to which velocity saturation affects the drain current and is within the range $1 \leq \alpha \leq 2$. In current sub-100 nm technologies, the device operates strongly under velocity saturation and therefore $\alpha \cong 1$. We assume that an ideal unit step input is applied to the circuit shown in Fig. 6. Writing the KCL at the nodes V_1 and V_2, we have

$$\text{KCL @} V_1 : i_d + C_1 \frac{dV_1}{dt} + \frac{V_1 - V_2}{R''} = 0 \qquad (17)$$

$$\text{KCL @V}_2 : \ C_2 \frac{dV_2}{dt} = \frac{V_1 - V_2}{R''} \tag{18}$$

where C_1 and C_2 are the wire sub-segment capacitances in Fig. 6. Simultaneous solving of (17) and (18) leads to a second order differential equation for the output voltage, V_{out} as

$$X\frac{d^2 V_{out}}{dt^2} + Y\frac{dV_{out}}{dt} + ZV_{out} = 0. \tag{19}$$

We have changed the variables in order to simplify the solution of the final differential equation in (19). The new variables, *X, Y,* and *Z,* are functions of the interleaved line parameters illustrated in Fig. 6. We have summarized these variables and their circuit-level parameters in Table 2. It is worth mentioning that $\mho_{d0}$ is the saturation conductance and is the essential α-power law model parameter used throughout this paper.

Table 2. Variables and equivalent parameters used for analytical methodology of dynamic delay.

Variable	Equivalent circuit-level parameters
$\mho_{d0}$	I_{d0}/V_{d0}
R'	$R_D + \beta R_W/2$
R''	$R_W/2$
C_1	$\beta(\delta_1 C_c + C_g)$
C_2	$(1-\beta)(\delta_2 C_c + C_g)$
X	$R''C_1 C_2$
Y	$C_1 + C_2 + \mho_{d0}R''C_2/(\mho_{d0}R' + 1)$
Z	$\mho_{d0}/(\mho_{d0}R' + 1)$

The linear equation in time domain can be written in Laplace form as

$$X(s^2 V_{out} - sv_{out}(0) - v_{out}'(0)) + Y(sV_{out} - v_{out}(0)) + ZV_{out} = 0. \tag{20}$$

Initial conditions indicate that the initial output voltage for a rising input should be the supply voltage V_{DD}, while the initial output voltage derivative is zero. Thus, the output voltage in Laplace form can be written as

$$V_{out}(s) = \frac{V_{DD}(Xs+Y)}{Xs^2 + Ys + Z} \tag{21}$$

The second-order differential equation in (19) has two real roots, making the interleaved system to operate over-damped. Although the time domain output voltage can be obtained using inverse Laplace transform of (21), we will employ some simplifications in the calculation of the propagation delay for the interleaved system shown in Fig. 6. The time domain output voltage of the interleaved system can be written in the form of

$$v_{out}(t) = a_1 e^{-s_1 t} + a_2 e^{-s_2 t} \tag{22}$$

where s_1 and s_2 are the roots of the characteristic equation of the interleaved system. The factors a_1 and a_2 can be calculated as

$$a_{1,2} = \frac{V_{DD}(-s_{1,2} + \frac{Y}{X})}{s_{2,1} - s_{1,2}}. \tag{23}$$

Taylor series expansion of the exponential functions is used here to approximate the functions of the output voltage under the assumption of $st \to 0$. Taylor series of an exponential function can be written as

$$e^{-st} = 1 - st + \frac{1}{2}s^2 t^2 \mp \cdots \tag{24}$$

Considering the first two terms in the Taylor series and ignoring the higher order terms, the dynamic propagation delay of our modified interleaved repeater insertion methodology, named as MIRIM, can be written as

$$D_{MIRIM}^{Dynamic} = \frac{0.5(1 + \mho_{d0}R')R''C_1 C_2}{(C_1 + C_2)(1 + \mho_{d0}R') + C_2\mho_{d0}R''}. \tag{25}$$

This delay is a function of the sub-segment capacitances which depends on the switching pattern of the neighbor lines. Based on (25), it is required to calculate the optimum relative position ratio, $\beta_{opt-MIRIM}$, to minimize the propagation delay in each bus line 1 and 2, illustrated in Fig. 5. While examining (25) and the switching factors mentioned in Table 1, we can show that there exists a certain value of $\beta_{opt-MIRIM}$ that leads to the minimization of the propagation delay equation while different switching factors are considered. This optimum position ratio can be calculated by equating the delay expression (25) for different switching factors, so as we obtain

$$\beta_{opt-MIRIM} = \frac{1}{2}(\sqrt{(2\eta+1)^2 + (2\gamma+1)^2 + 8\eta\gamma} - 2\eta - 2\gamma) \tag{26}$$

$$\eta = \frac{R_D}{R_W} \tag{27}$$

$$\gamma = \frac{1}{\mho_{d0}R_W}. \tag{28}$$

The optimum position ratio, $\beta_{opt-MIRIM}$, for the repeater-inserted lines in (26) is a function of the ratio of the repeater's output resistance to the segment's resistance and the ratio of the saturation resistance to the segment's resistance, γ. Substituting (26) in (25), the optimum (minimal) dynamic propagation delay is thus obtained as

$$D_{opt-MIRIM}^{Dynamic} = \beta_{opt}(1 - \beta_{opt})\frac{R_W}{4}(C_c + C_g). \tag{29}$$

The minimal propagation delay in (29) is independent of the switching patterns in Table 1 and thus it means that the adjacent lines appear as static lines. The resistance of the line dominates the repeater output resistance and the repeater saturation resistance in sub-100 nm technologies. The ratios η and γ approache zero and the propagation

delay varies quadratically with β_{opt} as demonstrated in (29). The variation of $\beta_{opt-MIRIM}$ with η and γ expressed by (26) is illustrated in Fig. 7.
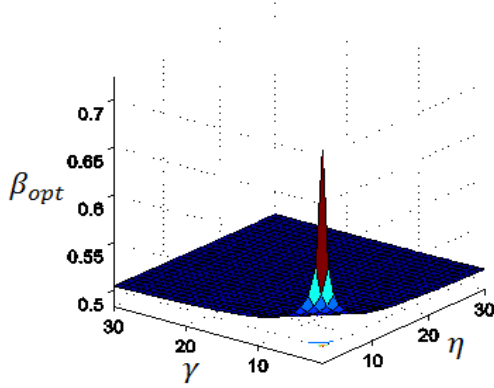

Fig. 7. Variation of $\boldsymbol{\beta_{opt-MIRIM}}$ with $\boldsymbol{\eta}$ and $\boldsymbol{\gamma}$

B. Static Propagation Delay Derivation

The static propagation delay of the interleaved line can be calculated by the same methodology mentioned in this section. Considering the circuit-level modeling of the interleaved repeater-inserted segment in Fig. 6, we now ignore the sub-segment capacitances of the line in order to derive an expression for the static signal propagation delay. Writing KCL at the nodes V_0 and V_{out}, we have

$$\text{KCL @} V_0 : i_d + C_{out}\frac{dV_0}{dt} + \frac{V_0 - V_{out}}{R_W} = 0 \tag{30}$$

$$\text{KCL @} V_{out} : C_L\frac{dV_{out}}{dt} = \frac{V_0 - V_{out}}{R_W} \tag{31}$$

Simultaneous solving of (30) and (31) leads to a second order differential equation for the output voltage, V_{out} as

$$X'\frac{d^2V_{out}}{dt^2} + Y'\frac{dV_{out}}{dt} + Z'V_{out} = 0. \tag{32}$$

Similarly, we introduce new variables in order to simplify the solution of the final differential equation in (32). The new variables $(X', Y',$ and $Z')$ and their circuit-level parameters are summarized in Table 3.

Table 3. Variables and equivalent parameters used for analytical methodology of static delay.

Variable	Equivalent circuit-level parameters
X'	$R_W{}^2 C_{out} C_L$
Y'	$R_W C_{out} + R_W C_L + \mho_{d0} R_W{}^2 C_L$ $/(1 + \mho_{d0} R_D)$
Z'	$\mho_{d0} R_W/(1 + \mho_{d0} R_D)$

Using the same strategy as the one used for the dynamic propagation delay calculation, we obtain the static propagation delay of the modified interleaved repeater-inserted segment as below

$$D_{MIRIM}^{Static} = \frac{0.5(1+\mho_{d0}R_D)R_W C_{out} C_L}{(C_{out}+C_L)(1+\mho_{d0}R_D)+\mho_{d0}R_W C_L}. \tag{33}$$

Eventually, the total propagation delay of the interleaved line using the methodology introduced in this section would be

$$D_{MIRIM} = D_{MIRIM}^{Static} + D_{MIRIM}^{Dynamic}. \tag{34}$$

C. Sensitivity Analysis

The sensitivity of the interleaved line considering the methodology introduced in this paper can easily be written as

$$S_t(\beta, l) = S_{t0} + \beta(1 - \beta)S_{tc} \tag{35}$$

where S_{t0} and S_{tc} are the static and dynamic sensitivity functions respectively. Additionally, S_{tc} can be written as

$$S_{tc} = 0.5r_W(c_c + c_g)l. \tag{36}$$

The optimum value of β approaches $1/\sqrt{2}$ in nano-technologies. Therefore, according to our methodology, the sensitivity of the optimum-placed interleaved segment to its length can be expressed as

$$S_t(\beta_{MIRIM}, l) \cong S_{t0} + \frac{\sqrt{2}-1}{4}S_{tc}. \tag{37}$$

Comparing the sensitivity functions for various repeater insertion strategies in (4), (6), (12), and (37), obviously it can be deduced that MIRIM has the least possible sensitivity to the segment length variations among all methodologies. We can also compare the sensitivity functions by

$$S_t(\beta_{MIRIM}, l) < S_{t-Hybrid} < S_t(\beta_{Interleaved}, l) < S_{t-Standard}. \tag{38}$$

4. Simulation Results and Discussions

The new proposed methodology was used to optimize the delay uncertainty in global interconnects, for verification purposes. As such, we applied it to coupled lines in various nanoscale technology nodes where the required parameters were based on ITRS (International Technology Roadmap for Semiconductors). Moreover, to verify our derivations, we have used various level-54 CMOS technologies to model the repeaters in SPICE. The ITRS technology parameters are shown in Table 4. The predictive technology model (PTM) [35] for the 65-nm, 45-nm, and 32-nm printed channel lengths is used, corresponding to the technology nodes described in ITRS [34]. R_{D0}, $\mho_{d0}$, C_{out0}, and C_{L0} were obtained via SPICE simulations. α_n and α_p are the saturation indices for NMOS and PMOS devices, respectively, and are determined employing the method described in [31]. Each wire sub-segment is modeled by the coupled $3\pi RC$ model to increase the accuracy of the proposed strategy. The optimum values for the segment length, repeater sizes, ratio of the output repeater resistance and the saturation resistance to the segment resistance as well as the optimum value for the relative position ratio, β_{opt}, are summarized in Table 5. The parameters l_{opt} and k_{opt} are calculated using (13) and (14).

Table 4. Technology and equivalent circuit model parameters for top layer metal for different technology nodes based on the ITRS 2008 [34].

Tech. node (nm)	65	45	32
Width (nm)	68	45	32
Spacing (nm)	68	45	32
Thickness (nm)	115	81	60
ILD (nm)	102	97	85
K_{ILD}	2.5	2.3	2.1
Length(mm)	3	3	3
r_W (KΩ/mm)	2.8	6	11.4
c_g (fF/mm)	26	18	13
c_c (fF/mm)	54	52	53
l(nH/mm)	2.42	2.5	2.5
α_n	1.03	0.91	0.86
α_p	1.12	1.05	0.98
R_{D0}(KΩ)	21	27	33
$\mho_{d0}$(μS)	86	34	30
C_{out0}(fF)	0.36	0.15	0.1
C_{L0}	0.46	0.16	0.09

Table 5. Optimum calculated values for different technology nodes.

Tech. node (nm)	65	45	32
l_{opt}(mm)	0.3	0.15	0.09
k_{opt}	46	58	61
η_{opt}	0.54	0.51	0.52
γ_{opt}	0.3	0.55	0.52
$\beta_{opt-Interleaved}$	0.61	0.61	0.61
$\beta_{opt-MIRIM}$	0.59	0.58	0.57

Considering the methodology proposed in this paper to reduce the delay uncertainty, busses of 3-mm length for various technologies are optimized to achieve the minimum worst case propagation delay.

The SPICE simulation results are presented in Fig. 8, where the worst case propagation delay is illustrated as a function of the relative position ratio for different sub 100-nm technologies. The simulation results clearly match the analytical derivation expressed in (26) which is mentioned in Table 5. It is worth mentioning that we not only have optimized the delay uncertainty caused by the capacitive coupling of the adjacent busses, but we also have minimized the absolute propagation delay value in our simulations considering the optimum value for η_{opt} and γ_{opt}.

The worst case propagation delay of the analyzed delay uncertainty reduction methodologies as a function of the normalized segment length for three sub 100-nm technologies is illustrated in figures 9, 10 and 11. In each case, the standard repeater insertion strategy has the maximum worst case propagation delay since it was previously shown in equation (2). Moreover, the proposed
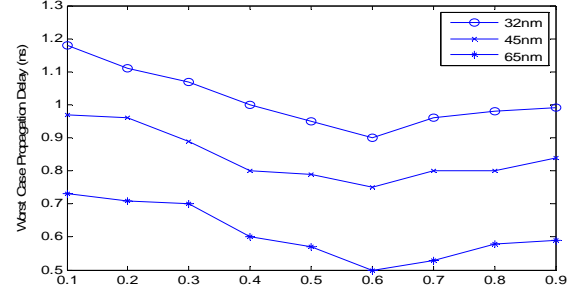

Fig. 8. Worst-case propagation delay using MIRIM for different CMOS and interconnect technologies.
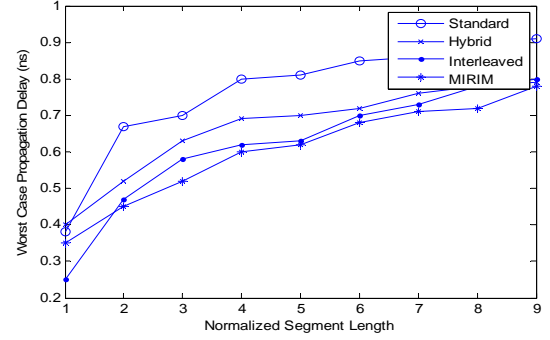

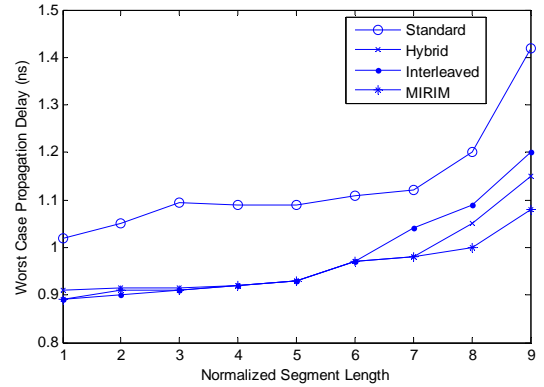Fig. 9. Worst-case propagation delay using different methodologies in 65-nm technology.

Fig. 10. Worst-case propagation delay using different methodologies in 45-nm technology.
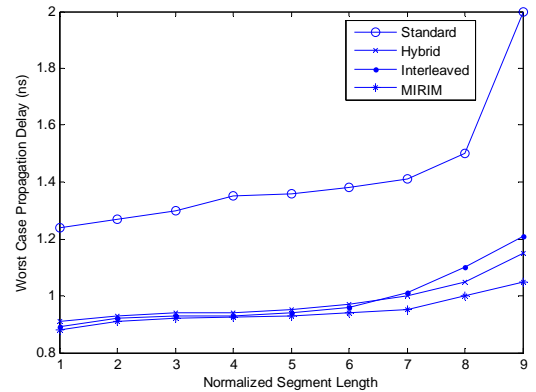

Fig. 11. Worst-case propagation delay using different methodologies in 32-nm technology.

method described in this paper presents the minimum simulated propagation delay among the analyzed strategies. The hybrid and interleaved lines exhibit different trends in each technology. It is also obvious that the standard repeater insertion has the maximum sensitivity to the segment length variations due to different target delays.

The average measured sensitivity of various repeater insertion methodologies using SPICE simulations is summarized in Table 6 for different sub 100-nm technologies. The proposed MIRIM achieves a maximum sensitivity reduction of 33% for 65-nm technology, 51% for 45-nm technology, and 34% for 32-nm technology node where the simulated results in Table 6 clearly verify our previous derivation in (38).

Delay uncertainty in interconnects is usually defined as the ratio of delay variation to the worst case delay and therefore, is written as [26]

$$\text{Uncertainty} = \frac{t_{\text{prop}}(\max) - t_{\text{prop}}(\min)}{t_{\text{prop}}(\max)}. \tag{39}$$

Here, $t_{prop}(\max)$ and $t_{prop}(\min)$ are the maximum and minimum propagation delay of the wire, respectively. Uncertainty ranges between 0 and 1 for the minimum and maximum possible uncertainty, respectively. Fig. 12 presents the simulated uncertainty as a function of normalized segment length variation in different technologies. Average simulated uncertainty is also summarized in Table 7 where our proposed MIRIM uncertainty is less than 0.1 for all technologies. This nonzero uncertainty is due to the mathematical simplifications used to optimize the relative position ratio, $\beta_{opt-MIRIM}$, in (26), since the first two terms in the Taylor series have been considered in the propagation delay expression. The proposed methodology achieves a

Table 6. Average simulated sensitivity of various methodologies for different technology nodes.

Tech. node (nm)	65	45	32
Standard (psec/mm)	180	130	256
Hybrid (psec/mm)	126	78	196
Interleaved (psec/mm)	183	109	261
MIRIM (psec/mm)	120	64	170

Table 7. Average simulated uncertainty of various methodologies for different technology nodes.

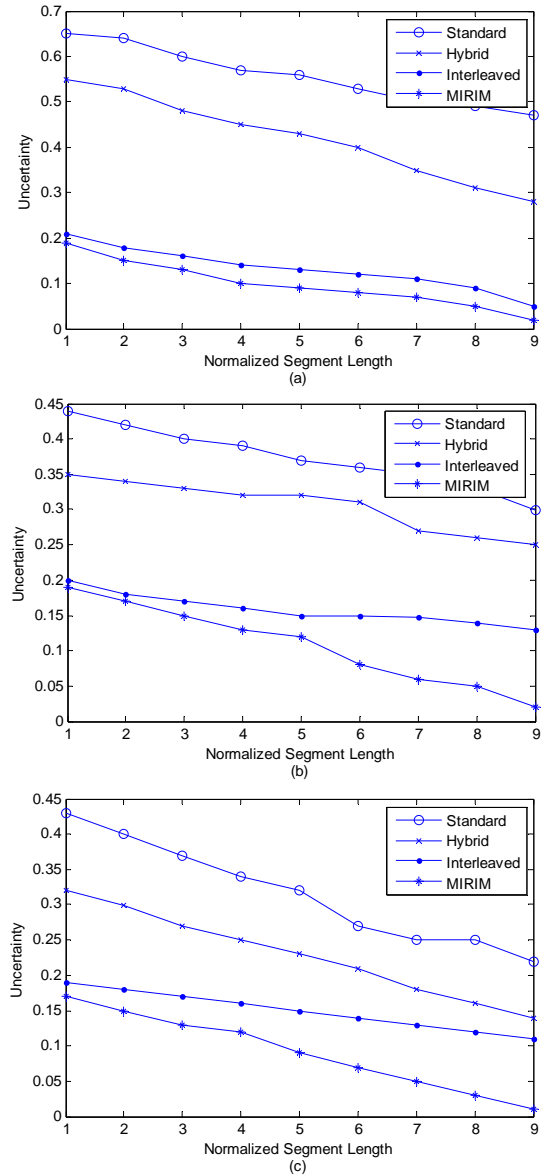| Tech. node (nm)	65	45	32
Delay Uncertainty in Standard	0.55	0.37	0.32
Delay Uncertainty in Hybrid	0.41	0.3	0.22
Delay Uncertainty in Interleaved	0.13	0.16	0.15
Delay Uncertainty in MIRIM	0.1	0.09	0.08

Fig. 12. Uncertainty as a function of normalized segment length for (a) 65-, (b) 45-, and (c) 32-nm technology.

maximum uncertainty reduction of 81% for 65-nm technology and 75% for 45-nm and 32-nm technology nodes in comparison with the standard bus configuration which has the maximum delay variation based on (2) and the SPICE simulation results. Moreover, MIRIM achieves a maximum uncertainty reduction of 63% and 46% for different simulated technology nodes in comparison with the hybrid polarity and classical interleaved bus configurations. As it is mentioned before in this section, all the simulations have been performed for the 3-mm bus for various analyzed strategies and in different technology nodes.

5. Conclusion

In this paper, a novel and accurate methodology for optimum interleaved-repeater positioning in global interconnects has been introduced. Comparing the analytical delay uncertainty for available repeater insertion techniques, an optimum value for the relative position ratio

of the interleaved line was extracted while new and efficient expressions were derived. The α-power law for MOS devices was used in the proposed model in order to increase the accuracy of the methodology. For reducing the maximum propagation delay of the transmitted signal in a global bus, the new positioning approach was proven to minimize the delay uncertainty caused by the coupling capacitance switching of the adjacent lines. The simulated uncertainty of the proposed methodology was less than 0.1 for all beyond 100-nm technology nodes. It has been also shown that the presented strategy offers lower propagation delay sensitivity to the segment length variations in comparison with previously used repeater insertion techniques. The proposed methodology has achieved a maximum sensitivity reduction of 33% for 65-nm technology, 51% for 45-nm technology, and 34% for 32-nm technology node. All the derivations have been verified using SPICE simulations considering the level-54 beyond 100-nm CMOS technologies. The significance and valuable benefit of the proposed delay uncertainty reduction method is more pronounced when we note that the ratio of the coupling capacitance to the total capacitance of the wire increases due to the continuous scaling in technology node.

References

[1] A. Ceyhan and A. Naeemi, "Cu interconnect limitations and opportunities for SWNT interconnects at the end of the roadmap," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 374-382, Jan. 2013.

[2] S. Tuuna, E. Nigussie, J. Isoaho, and H. Tenhunen, "Modeling of energy dissipation in RLC current-mode signaling," *IEEE Trans. VLSI Syst.*, vol. 20, no. 6, pp. 1146-1151, June 2012.

[3] E. A. Foreman, P. A. Habitz, M. C. Cheng, and C. Visweswariah, "A novel method for reducing metal variation with statistical static timing analysis," *IEEE Trans. Computer-Aided Des. Integr. Circuits Syst.*, vol. 31, no. 8, pp. 1293-1297, Aug. 2012.

[4] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits—A Design Perspective*, (2nd Ed.) McGraw-Hill, 2002.

[5] K. Hirose and H. Yassura, "A bus delay reduction technique considering crosstalk," in *Proc. Des. Autom. Test Eur. (DATE),* pp. 441–445, 2000.

[6] D. B. Jarvis, "The effects of interconnections on high-speed logic circuits," *IEEE Trans. Electron. Computers*, vol. EC-10, pp. 476–487, Oct. 1963.

[7] Y. I. Ismail and E. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 2, pp. 195–206, Apr. 2000.

[8] P. Zuber, O. Bahlous, T. Ilnseher, M. Ritter, and W. Stechele, "Wire topology optimization for low power CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 1, pp. 1–11, Jan. 2009.

[9] C. Duan, V. H. Cordero Calle, and S. P. Khatri, "Efficient on-chip crosstalk avoidance CODEC design," *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 17, no. 4, pp. 551–560, Apr. 2009.

[10] R. Kumar, "Interconnect and noise immunity design for the Pentium 4 processor," *Intel Technol. J.*, 2001.

[11] P. Chen, D. K. Kirkpatrick, and K. Keutzer, "Miller factor for gate-level coupling delay calculation," in *Proc. IEEE/ACM Int. Conf. Computer.- Aided Des. (ICCAD)*, pp. 68–74, Nov. 2000.

[12] P. Gupta and A. B. Kahng, "Wire swizzling to reduce delay uncertainty due to capacitive coupling," in *Proc. Int. Conf. VLSI Des.*, pp. 441–445, Jan. 2004.

[13] R. Arunachalam, E. Acar, and S. Nassif, "Optimal shielding/spacing metrics for low power design," in *Proc. IEEE Symp. VLSI*, pp. 167–172, Feb. 2003.

[14] K. Hirose and H. Yassura, "A bus delay reduction technique considering crosstalk," in *Proc. Des. Autom. Test Eur. (DATE)*, 2000, pp. 441–445.

[15] G. Chen and E. G. Friedman, "Low-power repeaters driving RC and RLC interconnects with delay and bandwidth constraints," *IEEE Trans. VLSI Syst.*, vol. 14, pp. 161–172, Feb. 2006.

[16] H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Trans. Electron Devices*, vol. 32, no.5, pp. 903-909, May. 1985.

[17] M. L. Mui, K. Banerjee,and A. Mehrotra, "A global interconnect optimization scheme for nanometer scale VLSI with implications for latency, bandwidth, and power dissipation," *IEEE Tran Electron Devices,* vol. 51, no. 2, pp. 195-203, Feb. 2004..

[18] M. Zangeneh and N. Masoumi, "An analytical delay reduction strategy for buffer-inserted global interconnects in VDSM technologies," in *Proc. 19th European Conf. on Circuit Theory and Design*, pp. 470-475, Aug. 2009.

[19] M. Zangeneh and N. Masoumi, "Throughput optimization for interleaved repeater-inserted interconnects in VLSI design," *3rd International Nanoelectronics Conf. (INEC10)*, pp. 1443-1444, Jan. 2010.

[20] V. Adler and E. G. Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 5, pp. 607–616, May. 1998.

[21] C. Alpert, A. Devgan, and S. Quay, "Buffer insertion for noise and delay optimization," *IEEE Trans. Comput.-Aided Des.Integr. Circuits Syst.*, vol. 18, no. 11, pp. 1633–1645, Nov. 1999.

[22] M. Ghoneima and Y. Ismail, "Optimum positioning of interleaved repeaters in bidirectional buses," *IEEE Trans. Computer-Aided Des. Integr. Circuits Syst.*, vol. 24, no. 3, pp. 461–469, Mar. 2005.

[23] H. Shah, P. Shiu, B. Bell, M. Aldredge, N. Sopory, and J. A. Davis, "Repeater insertion and wire sizing optimization for throughput-centric VLSI global interconnects," in *Proc. IEEE Int. Conf. Computer-Aided Design*, pp. 280–284, 2002.

[24] V. V. Deodhar and J. A. Davis, "Optimization of throughput performance for low-power VLSI interconnects," *IEEE Trans. VLSI Syst.*, vol. 13, pp. 308–318, Mar. 2005.

[25] R. Weerasekera, D. Pamunuwa, L. Zheng, and H. Tenhunen, "Minimal-power, delay-balanced SMART repeaters for global interconnects in the nanometer regime," *IEEE Trans. VLSI Syst.*, vol. 16, pp. 589–593, May. 2008.

[26] C. J. Akl and M. A. Bayoumi, "Reducing interconnect delay uncertainty via hybrid polarity repeater insertion," *IEEE Trans. VLSI Syst.*, vol. 16, pp. 1230–1239, Sep. 2008.

[27] V. Adler and E. G. Friedman, "Uniform repeater insertion in *RC* trees," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 10, pp. 1515–1523, Oct. 2000.

[28] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.

[29] B. S. Cherkauer and E. G. Friedman, "Design of tapered buffers with local interconnect capacitance," *IEEE J. Solid State Circuits*, vol. 30, pp. 151–155, Feb. 1995.

[30] N. C. Li, G. L. Haviland, and A. A. Tuszynski, "CMOS tapered buffer," *IEEE J. Solid State Circuits*, vol. 25. no. 4, pp. 1005-1008, Aug. 1990.

[31] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.

[32] W. C. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *J. Appl. Phys.,* vol. 19, no. 1, pp. 55–63, *Jan.* 1948.

[33] F. Rafiq, M. Chrzanowska-Jeske, H. H. Yang, and N. Sherwani, "Integrated floorplanning with buffer/channel insertion for bus-based microprocessor designs," in *Proc. Int. Symp. Phys. Design*, pp. 56–61, Apr. 2002.

[34] International Technology Roadmap for Semiconductors (ITRS), 2008.

[35] Predictive Technology Model (PTM) [Online]. Available: http://www.eas.asu.edu/~PTM/

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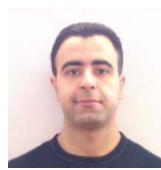
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