Investigation of a SiGe Tunnel FET: Comparison to Si and Ge TFETs

Mohammad Kamali Moghadam and Seyed Ebrahim Hosseini

Abstract. In this paper a SiGe $p^+n^+in^+$ tunneling transistor is studied and compared with Si and Ge based transistors. Moreover, in the proposed structure a δ-doped n^+ region is considered between the source and the channel, and this region is optimized in the sense of region width (Wd) and doping level for the highest ratio of on-current to off-current and the lowest sub-threshold swing. Simulations show that I_{on}/I_{off} ratio higher than 11 orders of magnitude and sub-threshold swing of 16.6 mV/dec, which is well below 60 mV/dec limit of conventional MOSFETs, are obtained.

Keywords: Tunnel FET, $\boldsymbol{I_{on}/I_{off}}$ ratio, band-to-band tunnelling, sub-threshold swing.

1. Introduction

Logic switching devices that operate based on band-to-band tunneling (BTBT) are considered as candidates for extremely low voltage operation (< 0.5 V) due to the potential for sub-60-mV/dec swing (at room temperature) over part of their current switching characteristic [1-9]. Efficient devices with large I_{on}/I_{off} ratio at low Vdd operation will require very low energy barrier for tunneling, sharp and high tunnel-junction doping concentration, and small effective gate-insulator thickness [8]. Recent measurements of strained-$Si_{0.6}Ge_{0.4}$ gated diodes with Eg = 0.7 eV have demonstrated a significant enhancement in the gate-controlled tunneling current relative to co-processed silicon control devices due to the narrow band gap material [7]. Moreover, the insensitivity of the measurements to temperature in the 77 to 300 K range and the agreement with simulation using a quantum–mechanical BTBT model confirmed the gate-controlled BTBT-based device operation in strained-SiGe devices [7]. In order to potentially improve the switching characteristics of tunneling FETs (TFETs), increased junction doping level and reduced energy barrier for tunneling are expected to be required [9].

Tunnel FETs (TFETs) which can exhibit sub-threshold swing (SS) lower than 60 mV/dec [10, 11] are interesting candidates for logic switching devices applications [12-14]. TFETs turn to on-state based on band to band tunneling (BTBT) [14-18] and have the potential for very low off current with a sub-threshold swing beyond 60 mV/dec limit of conventional MOSFETs [11, 19]. Various TFETs are investigated in the literature, for example, with gate overlap/underlap [20], strained channel [21] and high-k gate dielectric [22]. Although TFETs have low off-state current, on-state current is not acceptably high [23, 12]. This results in low I_{on}/I_{off} ratio (on the order of 10^3~10^6 [24]) which limits application of TFETs in digital circuits [20]. Therefore new TFET designs are needed in order to attain high I_{on}/I_{off} ratio. In order to increase on-state current a SiGe delta layer at the edge of the source [25], SiGe [25] and Ge [18] in the source region, double gate with a SiGe source [26] and high-k dielectric [20] is used. Using high-k gate dielectric improves on state current. Using Ge with a lower band gap as the source material improves I_{on}/I_{off} ratio significantly [18]. In order to increase on-state current, dual material gate TFET is also studied [27, 28]. The double gate architecture has been reported in [26]. In this paper a $p^+n^+in^+$ TFET with a δ-doped n^+ region at the source side is proposed and optimized for high I_{on}/I_{off} ratio and low sub-threshold swing.

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2. Device Structure

The tunnel FET structure in this paper has four regions ($p^+n^+in^+$) in which the source region is p^+ layer, the drain region is n^+ and the channel is intrinsic region (lightly doped p). In order to enhance tunneling, a δ-doped n^+ region is inserted at the beginning of the channel. The gate oxide and contact has a small overlap with the source and drain regions. Figure 1 depicts the tunnel FET structure studied in this paper. In this structure the width of the active layer is t_s=60 nm, the gate oxide and buried oxide thicknesses are t_{ox}=2.5 nm and t_{box}=100 nm, respectively. The δ-doped n^+ width is varied between W=1 nm and 5 nm in order to pursue the optimized W. The channel length is considered L_{ch}=100 nm, the source and the drain doping levels are 1×10^{20} /cm^3 and 2×10^{19} /cm^3, respectively, the channel doping is 10^{16} /cm^3, and δ-doped n^+ doping is 10^{19} /cm^3.

Simulations are performed using Atlas Silvaco device simulator, and analytic calculations according to tunneling equations are performed in Matlab environment. Analytic calculations are based on band to band tunneling (BTBT) model [8, 9]. The gate voltage is swept from 0 to 3 V. The transfer and the output characteristics and I_{on}/I_{off} ratio are studied.

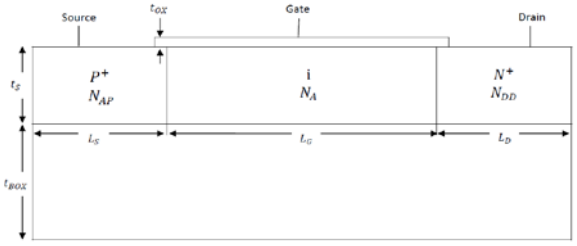

Fig. 1. Device structure of the pnin tunnel FET.

To optimize the device characteristics, the width of δ-doped n^+ region is varied from W=1 nm to 5 nm and the device characteristics are studied in order to optimize the width of this region. Also, the breakdown voltage in the output characteristics is investigated.

In order to investigate the device performance, extensive device simulations were performed using Atlas Silvaco device simulator. The tunneling calculations in our TFET were based on the well-known equations for tunneling current [30]

$$I_t = I_{(C\to V)} - I_{(V\to C)} = A\int_{E_C}^{E_V}\left[F_C(E) - F_V(E)\right]\times T_t(E)\,n_C(E)\,n_V(E)\,dE. \quad (1)$$

According to this equation, the drain current is proportional to the tunneling probability T(E), which is obtained as following [31]

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_S}{\varepsilon_{ox}}t_{ox}t_S}\right)\Delta\Phi \quad (2)$$

In this equation m* is the electron effective mass, E_g is band gap, ΔΦ is the energy range over which tunneling can take place, and t_{ox}, t_s, ε_{ox}, ε_s are the oxide and silicon films thicknesses and dielectric constants respectively, and ħ is the reduced Planck's constant.

3. Simulation Results

In Fig. 2 conduction and valance bands of the tunnel FET are depicted with W = 1 nm, V_{DS} = 0.5 V, and V_{GS} = 0 & 0.5 V. As this figure shows when the gate voltage is 0 V, there is no region for tunneling (i.e. there is no allowed energy levels for the electrons in the source valance band aligned with empty levels in the channel conduction band), but when the gate voltage is 0.5 V, the conduction band of the channel is lower than the valence band of the source. As a result, electrons of the source valance band can tunnel to the channel conduction band through the energy gap. We investigate device characteristics with different materials as the body region.

3.1. Si TFET

In this section we investigate silicon based TFET. The tunneling probability depends considerably on the value of W. Figure 3 shows the drain current versus V_{GS} at V_{DS}=0.5 and W varied from 1 nm to 5 nm. With a small W, the tunneling probability decreases which results in low off-current. On the other hand, with a large W, the tunneling probability increases which in turn increases the on-current. Increasing I_{on} is important in tunnel FETs [30]. On the other hand, with increasing W, at the same time, the off-current increases substantially which results in a low I_{on}/I_{off} ratio. Low I_{on}/I_{off} ratio prevents proper switching of the transistor from on- to off-state. It seems that W=1 nm is an optimum value for the δ-doped region width with a Si body.

As Fig. 4 shows, the I_{on}/I_{off} ratio reveals monotonic decrease up to W=5 nm, after which this ratio remains essentially constant. At W=1 nm the I_{on}/I_{off} ratio is about 9 orders of magnitude, which is comparable to conventional MOSFETs. Moreover, as Fig. 5 reveals, it seems at W = 1 nm the best value of sub-threshold swing is obtained.

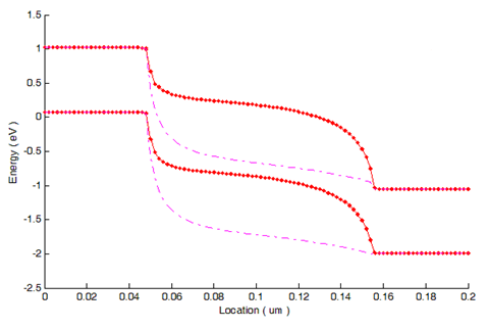

Fig. 2 . Energy bands diagram for W=1 nm, V_{DS} = 0.5 V, V_{GS} = 0 and 0.5 V.

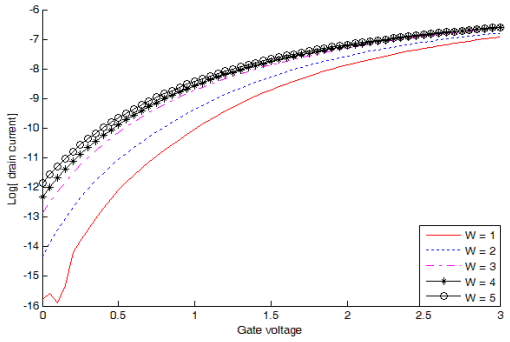

Fig. 3. Drain current versus V_{GS} for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with Silicone active region.

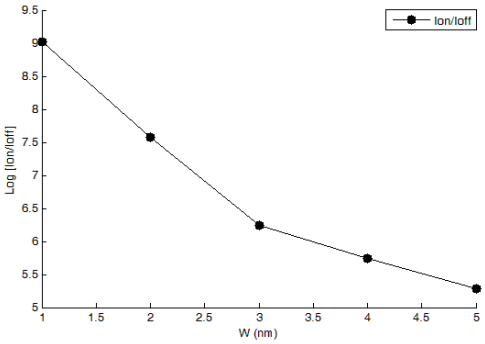

Fig. 4. I_{on}/I_{off} ratio for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with silicone active region.

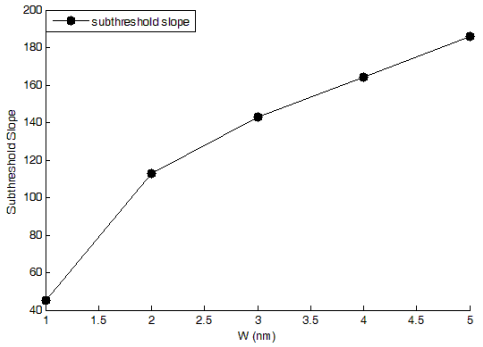

Fig. 5. Sub-threshold Swing (SS) for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with silicone active region.

3.2. Ge TFET

As it is observed in Figs. 6, 7, and 8, when Ge is used as TFET active region, device characteristics are optimized at W_d = 4 nm. Moreover it is seen that Si as active is superior than Ge.

3.3. SiGe TFET

Figs. 9 to 11 depict simulation results of $Si_{0.6}Ge_{0.4}$ TFET for W=1 to 5 nm. Comparing to Si- and Ge TFET results, it is evident that $Si_{0.6}Ge_{0.4}$ tunnel FET shows higher I_{on}/I_{off} ratio and lowest sub-threshold swing.

The n^+ pocket at the source-channel junction enhances the carrier tunneling. Therefore the PNPN tunnel FET has better performance than TFET without n^+ pocket. Figure 11 shows that the $Si_{0.6}Ge_{0.4}$ tunnel FET has better sub-threshold swing than Si and Ge TFETs. It means the barrier height and tunneling width is reduced in the TFET with SiGe as the active region.

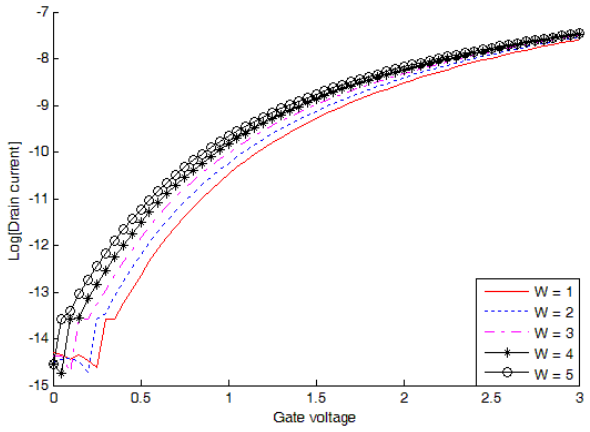

Fig. 6. Drain current versus V_{GS} for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with Ge active region.

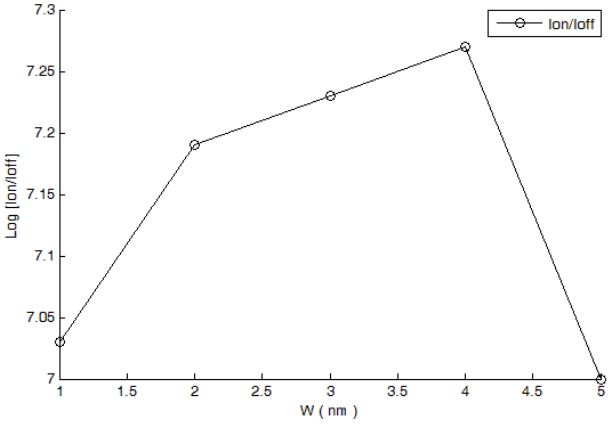

Fig. 7. Ion/Ioff ratio for W=1, 2, 3, 4, 5 nm and V_{DS}= 0.5 V with Ge active region.

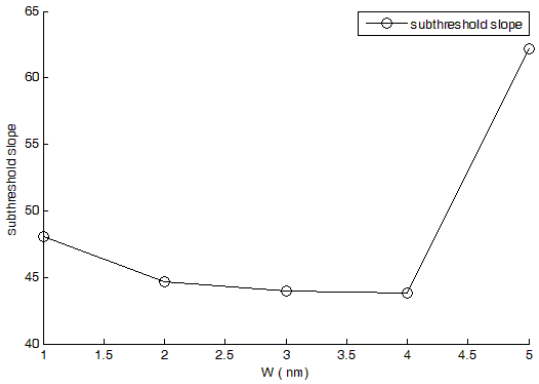

Fig. 8. Sub-threshold Swing (SS) for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with Ge active region.

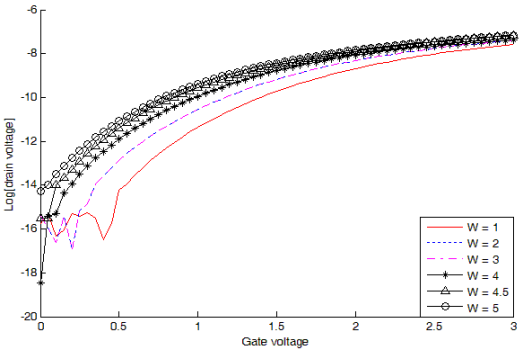

Fig. 9. Drain current versus V_{GS} for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with SiGe active region.

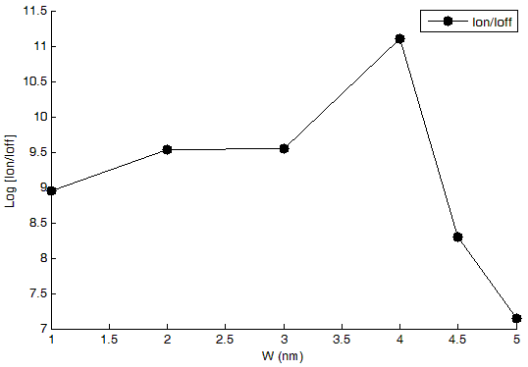

Fig. 10. Ion/Ioff ratio for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with SiGe active region.

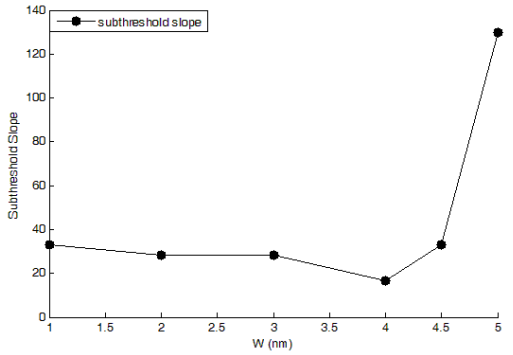

Fig. 11. Subthreshold Swing (SS) for W=1 , 2 ,3 , 4, 5 nm and V_{DS}= 0.5 V with SiGe active region.

4. Conclusion

Logic applications demand for transistors with low voltage, high I_{on}/I_{off} and low sub-threshold swing. As it is clear from obtained results in this paper, SiGe tunnel FETs with a 4 nm width δ-doped region, exhibit I_{on}/I_{off} of more than 11 orders and SS= 16.6 mV/dec, which are suitable for logical circuits with power supply of 0.5 V.

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