Low-Power Level-Shifting Architecture for Sub-threshold Logic Circuits

Seyed Rasool Hosseini, Mehdi Saberi, and Reza Lotfi

Abstract. This paper presents a power-efficient voltage level shifter converting low levels of input voltages (sub-threshold) to high levels of the output voltages (above threshold). In order to reduce the existing contention in the output nodes between pull-up and pull-down devices, the proposed circuit uses a current generator to reduce the strength of the pull-up device when the pull-down device is pulling down the output node. This causes the circuit to be functional even for the sub-threshold input voltages. In order to avoid the static power dissipation, this current generator turns on only during the transition times in which the logic level of the input signal is not corresponding to the output logic level. Simulation results of the proposed circuit in a 0.18-µm technology confirm that for a low supply voltage of $V_{DDL} = 0.42\ V$ at the input and a high supply voltage of $V_{DDH} = 1.8\ V$ at the output, the level shifter has a propagation delay of *22 ns*, an energy per transition of *340 fJ*, and a static power dissipation of *0.42 nW* for 1-M Hz input signal.

Keywords: Level shifter, level converter, sub-threshold, low power operation, dual supply.

1. Introduction

Lowering the supply voltage is one of the most effective ways to reduce both dynamic and leakage powers of digital circuits [1]-[5]. In this way, in order to greatly decrease the power consumption, the value of the supply voltage is chosen to be less than the threshold voltage of the devices. On the other hand, reducing the supply voltage increases the circuit propagation delay and therefore reduces the performance of the circuit [6]. In order to avoid the speed reduction, multi-supply systems have been proposed [7]. In this way, a low supply voltage (*i.e.* V_{DDL}) is applied to the digital blocks on the noncritical paths while a high supply voltage (*i.e.* V_{DDH}) is applied to the high-speed logic gates. A major problem in multi-supply systems is the conversion of the lower logical levels of (0, V_{DDL}) to the higher logical levels of (0, V_{DDH}). In order to overcome this problem, level-converting or level-shifting circuits have been presented [8]-[15]. It should be noted that the use of the level shifter results in an increase in the power consumption, the propagation delay, and the area occupation of the system [7]. Hence, design of power-efficient level shifters with minimum propagation delay and small area is of the interest of the *VLSI* circuit community. Moreover, the level shifter must be able to operate correctly even for low values (*i.e.* sub-threshold) of the input signal. Therefore, in literature, several attempts have been made to improve the performance of the level shifters [8]-[10] to be discussed in Section 2.

The rest of the paper is organized as follows. In Section 2, recently presented high-performance level-shifting circuits are reviewed. Section 3 presents the proposed structure which is able to convert sub-threshold voltages with low power consumption. The circuit-level simulation results confirming the efficiency of the proposed circuit are presented in Section 4. Finally, the paper is concluded in Section 5.

2. Related Works

One of the conventional implementations of a level-shifting circuit is shown in Fig. 1. The operation of this circuit is as follows. When the input signal (*i.e. IN*) changes from "low" to "high", M_{N2} is turned off and M_{N1} is turned on trying to pull down the node Q_B. Consequently, M_{P2} is gradually turned on to pull up the node Q and to turn M_{P1} off. It is clear that there is a contention between the pull-up (*i.e.* M_{P1}) and the pull-down (*i.e.* M_{N1}) transistors during the transition times in which the output is not corresponding to the logic level of the input. This leads to increase in the propagation delay and therefore the power consumption of the circuit. Moreover, for sub-threshold values of the input signal, the pull-down transistor cannot discharge the node Q_B because its current is much smaller than that of the pull-up transistor [15].

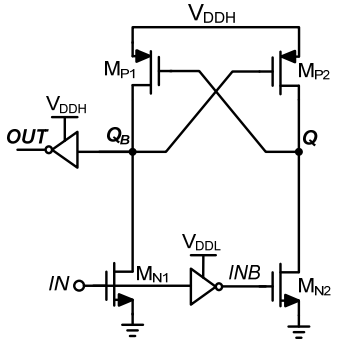

Fig. 1. The schematic of the conventional level shifter.

Manuscript received May 29, 2014; revised August 2, 2014; accepted August 16, 2014.
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In order to solve this problem, several approaches have been presented. Out of these, reducing the strength of the pull-up device is the most efficient approach [8]-[15]. In [8], two reduced-swing inverters (RSI) are employed to reduce the drive voltage of the pull-up transistors (*i.e.* M_{P1} and M_{P2}), as shown in Fig. 2(a). The conducting voltage of PMOS transistors is limited to $2V_{th}$ where V_{th} is the threshold voltage of diode connected transistors (*i.e.* M_{p4} and M_{p5}). Therefore, the strength of the pull-up transistors (M_{P1}, M_{P2}) is reduced and consequently the pull-down transistors will be able to pull the output node down. However, the area of this circuit increases because of the increased count of transistors. Moreover, the additional inverters and RSI circuits consume a significant amount of power [9].

Another structure, presented in [9], is shown in Fig. 2(b). In this circuit, two diode connected PMOS transistors (*i.e.* M_{P3} and M_{P4}) are inserted between the drains of NMOS and PMOS transistors. This causes a reduction in the drain voltage of NMOS transistors making them capable of pulling down the output node for the low values of the input voltages. It should be noted that in this structure, the gate-source voltage of the diode-connected transistors (*i.e.* M_{P3} and M_{P4}) is only half of the value of that of the level shifter shown in Fig. 2(b) leading to further reduction in the strength of the pull-up transistors. Therefore, this circuit will be able to operate with higher speed and smaller value for the minimum acceptable input voltage [9]. However, in steady state, a static current flows in this circuit because the gate-source voltage of the pull-up transistors are slightly above zero due to the voltage drop across the diode connected transistors.

Fig. 2(c) shows another circuit reported in [10]. In this circuit, in order for the circuit to work properly across all process/temperature corners, several methods such as sizing, threshold voltage selection, and diode-based voltage degradation have been utilized. This circuit consists of two main stages. The first stage is a cross-coupled differential inverter with a diode connected NMOS transistor (*i.e.* M_{N5}). The diode connected transistor is used to reduce the strength of the pull-up transistors. However, the swing of this stage is V_{DDH}-V_{th}. To solve this problem, the second stage uses a cross-coupled differential inverter for having full swing at the final output node. It should be noted that using two-stage design increases the propagation delay, which in turn increases the power consumption. Moreover, as in the conventional structure, there is a contention between the pull-up and pull-down transistors of the second stage, leading to even further increase in both the delay and the power consumption [14].

3. Proposed Level Shifter

In order to reduce the mentioned contention between the pull-up and pull-down devices, the proposed circuit, shown in Fig. 3 uses two current generators (*i.e.* M_{P3}, M_{P4}, M_{P5}, M_{P6}, M_{N3}, M_{N4}, M_{N5}, and M_{N6}) to reduce the strength of the pull-up device when the pull-down device is pulling down the output node. This causes the propagation delay and therefore the power consumption be reduced. Moreover, the pull-down device will be able to discharge the output node for sub-threshold input voltages. The operation of the proposed circuit is as follows. When the input signal is changed from "low" to "high", M_{N2} is turned off and M_{N1} is turned on trying to pull down the node Q_B. During the interval which Q_B is not corresponding to the logic level of the input, both M_{N6} and M_{N5} turn on and therefore a transition current flows through M_{N5}, M_{N6}, and M_{P5}. This current is mirrored into M_{P6} (*i.e.* I_1) and charges the node Q. Charging the node Q, reduces the gate-source voltage and therefore the strength of M_{P1}. Thus, the aforementioned contention between the pull-up and the pull-down devices is reduced and consequently M_{N1} will be able to pull down the node Q_B with less delay and power consumption. At the same time, in the other side of the circuit, M_{N3} turns off because $INB=V_{SS}$ and therefore there is no current flowing through M_{N4}, M_{N3}, and M_{P3}. Finally, when Q_B is pulled down, M_{N6} is turned off and therefore, no static current flows through M_{N6}, M_{N5}, and M_{P5}. This means that the current-generator structures are turned on only during the transition times in which the input and the output signals do not correspond avoiding the static power dissipation. As for the "high" to "low" transition of the input signal, the operation is forced to reverse states.

The input and the output signals and also the current waveforms of the current generators are shown in Fig. 4. It can be observed that both currents of I_1 and I_2 are only supplied to the nodes Q and Q_B during the transition times in which the logic level of the output signal is not corresponding to that of the input signal. Moreover, it should be noted that during the transition times, the current generator applies a transition current into either M_{P4} or M_{P6}

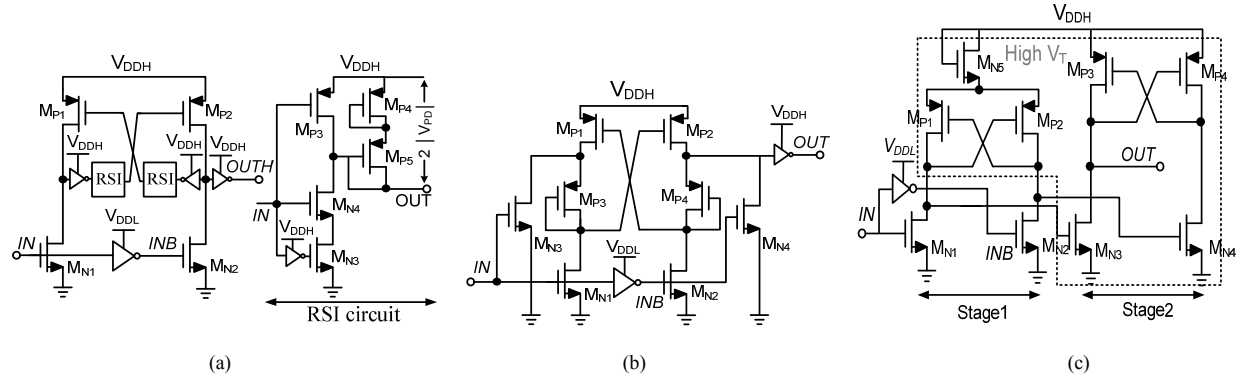

Fig. 2. Schematic of (a) the sub-threshold level shifter [8], (b) the level shifter presented in [9], and (c) the level shifter presented in [10].

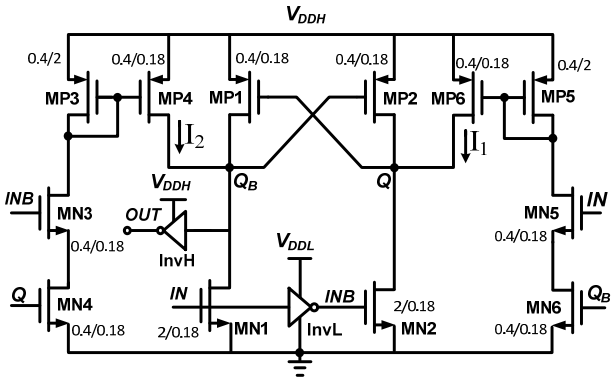

Fig. 3. Schematic of the proposed level shifter.

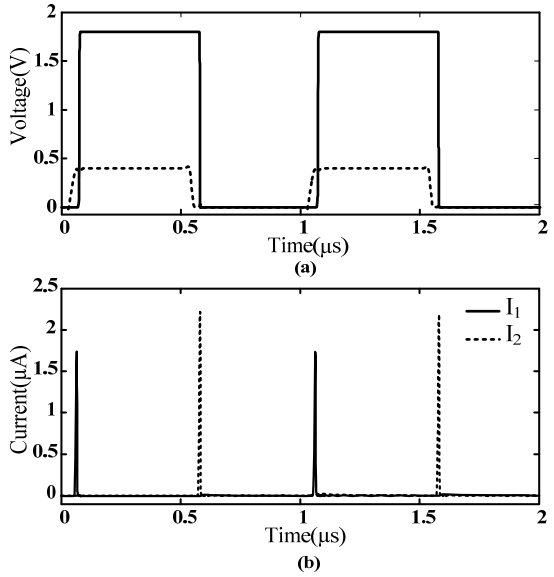

Fig. 4. Simulated waveforms of (a) the input and the output voltage, and (b) the current signals of the current generators.

(the one supposed to pull up the related output node) and no current is applied to the other branch, the output node of which is being pulled down by the pull-down device. Thus, the mentioned contention is reduced and therefore the proposed voltage level shifter not only is capable to convert low levels of the input voltages, but also its propagation delay and power dissipation are decreased.

4. Simulation Results

In order to verify the efficiency of the proposed level shifter, the proposed structure and also the structures presented in [9]-[11] have been simulated at transistor level in a 0.18-μm 1P6M CMOS technology. All circuits have been optimally designed to be functional in all process, voltage, and temperature (PVT) corners for V_{DDH} = *1.8 V*, V_{DDL} = *0.4 V* and the input frequency of 1 MHz so that they have minimum power consumption and silicon area. Therefore, the minimum sizes are chosen for the devices. In the proposed circuit, the transition current of I_1 and I_2 must be large enough to reduce the existing contention between

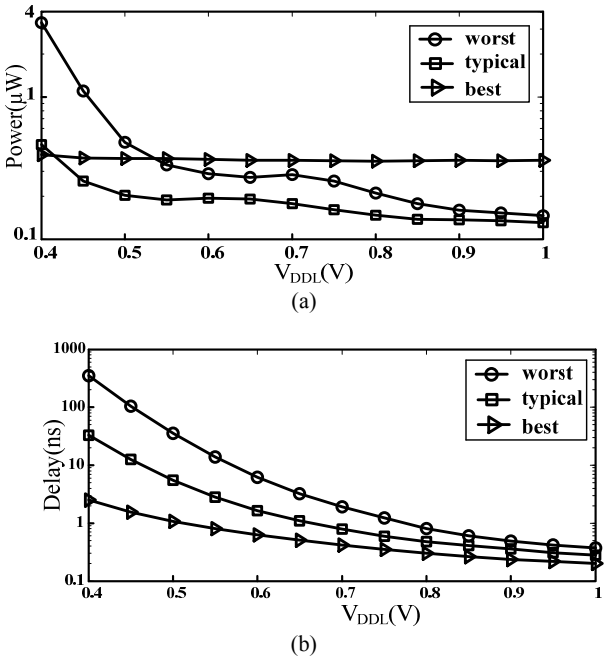

Fig. 5. Simulated values of (a) the power consumption and (b) the propagation delay of the proposed level shifter for different value of V_{DDL}. The value of input signal frequency is 1MHz.

the pull-up and the pull-down devices. On the other side, the power consumption of the auxiliary branches (*i.e.* M_{N5}, M_{N6}, and M_{P5}, and also M_{N3}, M_{N4}, and M_{P3}) should be minimized. Therefore, the current mirror ratio (*i.e.* M_{P4}/M_{P3} and M_{P6}/M_{P5}) should be more than one. For this purpose, the lengths of M_{P5} and M_{P3} are selected 2 μm whereas the lengths of the other transistors are minimum sizes (*i.e.* 0.18 μm). Moreover, the input NMOS transistors (*i.e.* M_{N1} and M_{N2}) must be somewhat strong to be able to pull the output node down even for the sub threshold input voltages. Hence, the widths of these NMOS transistors are chosen 2 μm while the size of the other transistors are minimum sizes (*i.e.* 0.4 μm).

In order to have a fair comparison between the structures, an inverter is added as a load circuit to all structures and the calculated power dissipation includes the power consumption of the load. In the proposed structure, the typical case includes typical-NMOS and typical-PMOS transistors, a high supply voltage of V_{DDH} = *1.8 V*, and a temperature of 25°C. Simulation results show that slow-NMOS and slow-PMOS result in the maximum delay. Moreover, a low temperature implies smaller device current. Therefore, slow-NMOS, slow-PMOS, a high supply voltage of V_{DDH} = *1.8 + 10% = 1.98 V*, and a temperature of 0°C were assumed as the worst case. Finally, a fast-NMOS, fast-PMOS, a high supply voltage of V_{DDH} = *1.8 - 10% = 1.62 V*, and a temperature of 120°C were chosen as the best case. Fig. 5 shows the simulation results of the propagation delay and also the total power consumption of the proposed circuit as a function of V_{DDL}, for typical, best, and worst cases. Although at V_{DDL} = *0.4 V*, the worst case delay and power dissipation are *137.2* and *8.5* times higher than the best case, the circuit still operates correctly at all PVT corners for 1-MHz input frequency. In order to investigate the operation of the proposed level shifter against the mismatch of the devices, a

4000-point Monte-Carlo simulation has been performed for $V_{DDH} = 1.8\ V$ and $V_{DDL} = 0.4\ V$ with both local and global variations. The results are shown as histograms of the propagation delay and the power dissipation in Fig. 6. As expected, the propagation delay has a log-normally distribution in the sub threshold region [11]. The normalized standard deviation values (σ/μ) of the delay and the power consumption are *0.53* and *0.27*, respectively. Moreover, simulation results show that the minimum values of V_{DDL} for which the circuit operates correctly at 100 Hz and 100 MHz are *0.08 V* and *0.55 V*, respectively for $V_{DDH} = 1.8\ V$.

Now, in order to compare the proposed level shifter with the other published works, Fig. 7 shows the simulated values of the power consumption and the propagation delay of the proposed structure and the circuits presented in [9]-[11] for different values of V_{DDL}. All structures have been simulated at the typical PVT case with a high supply voltage of V_{DDH} = 1.8 V. Moreover, Table 1 summarizes the performance of the proposed level shifter and compare it with other state-of-the-art works. It can be seen that the proposed voltage level shifter presents a good performance compared with the other architectures, especially from the power dissipation viewpoint.

Table 1. Performance Summary and Comparison.

	Technology	V_{DDH} (V)	$V_{DDL,minimum}$ (V)	Delay (ns)	Energy per transition (pJ)	Static power (nW)	Simulation/ Measurement
[9]	0.18 μm	1.8	0.13	10000 @ 0.2V	300@0.2V-100KHz	N.A.	Measurement
[10]	0.13 μm	1.2	0.18	57.9@0.2V	N.A.	N.A.	Measurement
[11]	90 nm	1	0.1	18.4@0.2V	0.094@0.2V-1MHz	6.62@0.2V	Pre-layout
[12]	0.13 μm	1.2	0.1	50@0.2V	25@0.2V@50KHz	8@0.2V	Measurement
[13]-DSLS1b	0.25 μm	1.2	0.35	252@0.35	52@0.35-N.A.	N.A.	Pre-layout
This work	0.18 μm	1.2	0.3	32.6@0.4V	0.074@0.4V-1MHz	0.164@0.4V	Pre-layout
		1.8	0.23	1770@0.23V	30.1@0.23V-100kHz	0.421@0.23V	

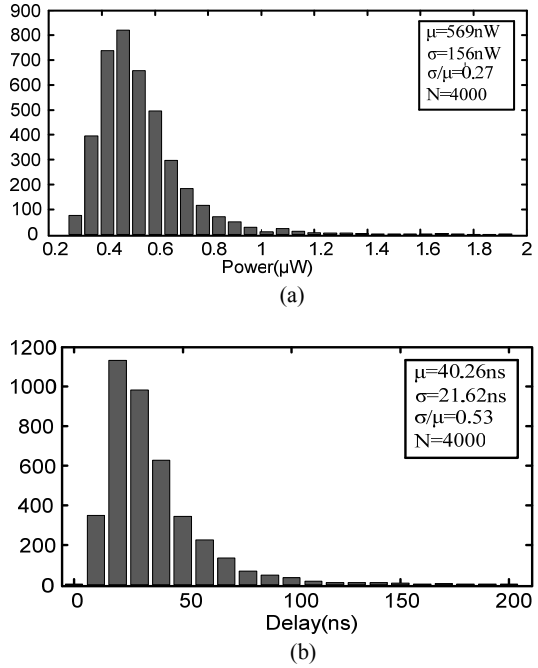

Fig. 6. Distribution of (a) the power dissipation and (b) the propagation delay of the proposed level shifter.

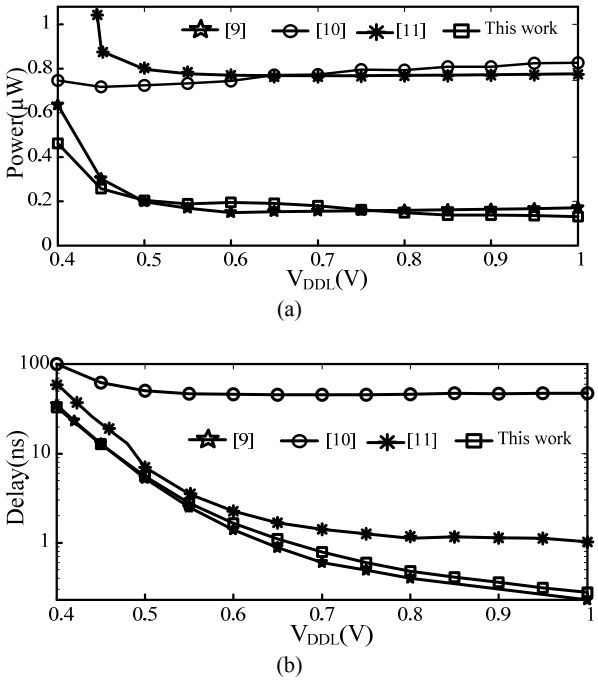

Fig. 7. Simulated values of (a) the total power dissipations and (b) the delays of the level-shifter circuits as a function of V_{DDL} at $V_{DDH} = 1.8\ V$. The employed value of the input frequency is 1 MHz.

Conclusions

In this paper, in order to convert low levels of input voltages to high levels of the output voltages, a low-power voltage level shifter has been presented. The proposed circuit decreases the strength of the pull-up device when the pull-down device is pulling down the output node. Not only the power consumption of the proposed circuit is decreased but also the circuit supports a wide voltage and frequency conversion range.

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