

Analysis on Radio-Frequency Modeling of Double- and Single-Gate Square-Shaped Extended Source TFETs

Saeid Marjani and Seyed Ebrahim Hosseini

Abstract. In this paper, the radio-frequency (RF) performances and small-signal parameters of double-gate (DG) square-shaped extended source tunneling field-effect transistors (TFETs) are investigated and compared with those of single-gate (SG) square-shaped extended source TFETs in terms of their cut-off and maximum oscillation frequencies and small-signal parameters. By using of a nonquasi-static (NQS) radio-frequency model, the small-signal parameters have been extracted. The results show that the DG square-shaped extended source TFET has higher transconductance, cut-off and maximum oscillation frequencies than single gate structure. The modeled Y-parameters are in close agreement with the extracted parameters for high frequency range up to the cut-off frequency. Results suggest that the DG square-shaped extended source TFETs seem to be the most optimal ones to replace MOSFET for ultralow power applications and RF devices.

Keywords: Double-gate (DG), radio-frequency (RF), nonquasistatic (NQS), extended source, tunneling field-effect transistor (TFET).

1. Introduction

Over the last decades, the tunnel field effect transistors (TFETs) with gate controlled band-to-band tunneling (BTBT) are investigated as a promising candidate to replace conventional metal-oxide-semiconductor field effect transistors (MOSFETs) for low-standby power (LSTP) and high-frequency applications. The unique and advantageous features of TFET are steep sub-threshold slope (SS), low power consumption and a very low leakage current [1]-[5]. Several works have addressed recently the devices with SS below 60 mV/decade at room temperature, both theoretically and experimentally [6]-[8]. However, all of them exhibit a minimized sub-threshold swing with a low OFF-current; their low ON-current was problematic. Consequently, it is necessary to improve the ON-current. There is a dramatic increase in the number of publications discussing the various designs to improve the ON-current by means of using band-gap engineering [9]-[15], small band-gap materials [16], [17], high-k dielectric materials [18], pocket doping [19]-[21], line-edge roughness [22], [23], vertical direction tunneling [24] and extended source [25].

Although there have been reports on the design and optimization of square-shaped extended source structure for better performance in terms of sub-threshold swing and drive current due to its enhanced tunneling area and total band-to-band generation [25], [26], their RF characterization and modeling have been seldom reported.

The goal of this paper is to determine the RF performances and small-signal parameters of double-gate (DG) square-shaped extended source TFETs and compared with single-gate (SG) square-shaped extended source TFETs. By using of the analytical equations for the Y-parameters of a nonquasi-static (NQS) radio-frequency model, the small-signal parameters were extracted for analysis of cut-off frequency, maximum oscillation frequency, gate-source capacitance, gate-drain capacitance and transconductance. This paper is organized as follows. After discussing in Section 2 the device structures and radio-frequency model of extended source TFETs, we present in Section 3 comparisons of RF performances and small-signal parameters of devices reported in the literature. We summarize our findings in Section 4.

2. Device Structure and Radio-Frequency Model of Extended Source TFETs

The cross-sectional views of double- and single-gate square-shaped extended source TFET devices used in the two-dimensional device simulation [27] are shown in Fig. 1(a) and (b), respectively. The p⁺ source and n⁺ drain are doped at 10²⁰ cm⁻³. The p-type body doping is 10¹⁵ cm⁻³. The gate oxide thickness, channel length and extended source length are 2, 30 and 10 nm, respectively. By using of a dynamic nonlocal path tunneling approach, band-to-band tunneling has been modeled. For higher accuracy band-gap narrowing, Shockley-Read-Hall recombination, mobility, Auger recombination and trap-assisted tunneling models are also activated [28]-[30].

Fig. 2 shows the transistor nonquasi-static model used to extract the small-signal parameters of the square-shaped extended source TFETs in this paper. R_g , C_{gs} , C_{gd} , C_{sd} , τ , g_m , and g_{ds} are the effective gate resistance, gate-source capacitance, gate-drain capacitance, source-drain capacitance, the charge transport delay, transconductance and source-drain conductance, respectively. The Y-parameters of the NQS model for the low-frequency region can be expressed as follows [31]:

$$Y_{11} = \frac{\omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega(C_{gs} + C_{gd})}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} \quad (1)$$

Manuscript received April 21, 2014; revised February 7, 2015; accepted February 20, 2015.

The authors are with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Iran. The corresponding author's email is: ehosseini@um.ac.ir.

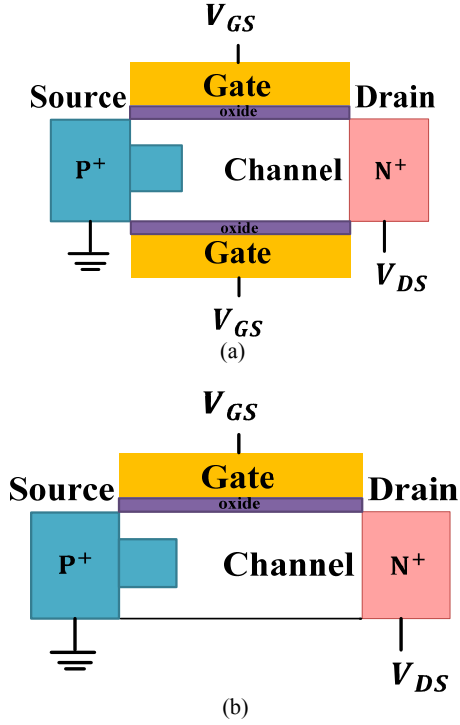


Fig. 1. Cross-section views of the (a) DG square-shaped extended source TFET, (b) SG square-shaped extended source TFET.

$$Y_{12} = \frac{-\omega^2 R_g C_{gd} (C_{gs} + C_{gd}) - j\omega C_{gd}}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} \quad (2)$$

$$Y_{21} = \frac{-j\omega C_{gd} - \omega^2 R_g C_{gd} (C_{gs} + C_{gd})}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} + \frac{g_m - j\omega g_m [\tau + R_g (C_{gs} + C_{gd})] - \omega^2 R_g g_m \tau (C_{gs} + C_{gd})}{[1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2] (1 + \omega^2 \tau^2)} \quad (3)$$

$$Y_{22} = g_{ds} + j\omega (C_{gd} + C_{sd}) + \frac{\omega^2 R_g C_{gd}^2}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2} + \frac{j\omega R_g g_m C_{gd} + \omega^2 R_g g_m C_{gd} [\tau + R_g (C_{gs} + C_{gd})]}{[1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2] (1 + \omega^2 \tau^2)} \quad (4)$$

In order to extract the small-signal parameters appropriate for low-frequency region, assumptions that $\omega^2 R_g^2 (C_{gs} + C_{gd})^2 \ll 1$ and $\omega^2 \tau^2 \ll 1$ have been used [31]. However, the validity of the assumptions will be checked by using the extracted parameters. Consequently, the equations of Y -parameters can be approximated into simple forms as follows [31]:

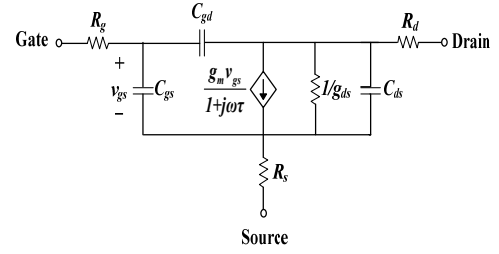


Fig. 2. Nonquasi-static equivalent circuit of a transistor to extract small-signal parameters of square-shaped extended source TFETs by the Y -parameter analysis.

$$Y_{11} \approx \omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega (C_{gs} + C_{gd}) \quad (5)$$

$$Y_{12} \approx -\omega^2 R_g C_{gd} (C_{gs} + C_{gd}) - j\omega C_{gd} \quad (6)$$

$$Y_{21} \approx g_m - \omega^2 R_g (C_{gs} + C_{gd}) (C_{gd} + \tau g_m) - j\omega [C_{gd} + \tau g_m + g_m R_g (C_{gs} + C_{gd})] \quad (7)$$

$$Y_{22} \approx g_{ds} + \omega^2 R_g C_{gd} \{C_{gd} + g_m [\tau + R_g (C_{gs} + C_{gd})]\} + j\omega [C_{gd} + C_{sd} + R_g g_m C_{gd}] \quad (8)$$

The small-signal parameters governing the RF behaviors can be extracted by using real and imaginary parts of equations (5)-(8) and the Y -parameters from the simulation results. The parameters of g_m , g_{ds} , R_g , C_{gd} , C_{gs} , C_{sd} , and τ are expressed as follows [31]:

$$g_m = \text{Re}[Y_{21}] \Big|_{\omega=0} \quad (9)$$

$$g_{ds} = \text{Re}[Y_{22}] \Big|_{\omega=0} \quad (10)$$

$$R_g = \frac{\text{Re}[Y_{11}]}{(\text{Im}[Y_{11}])^2} \quad (11)$$

$$C_{gs} = \frac{\text{Im}[Y_{11}] + \text{Im}[Y_{12}]}{\omega} \quad (12)$$

$$C_{gd} = -\frac{\text{Im}[Y_{12}]}{\omega} \quad (13)$$

$$\tau = -\frac{\frac{\text{Im}[Y_{12}]}{\omega} + C_{dg} + g_m R_g (C_{gs} + C_{gd})}{g_m} \quad (14)$$

$$C_{sd} = \frac{\text{Im}[Y_{22}]}{\omega} - C_{gd} - R_g g_m C_{gd} \quad (15)$$

The cut-off and maximum oscillation frequencies of TFETs have been obtained from the high-frequency current gain and unilateral power gain data of the TCAD simulation, respectively. Extracted small-signal parameters from TCAD simulation have been used for the evaluation of the RF performances.

3. Results and Discussion

Fig. 3 shows the gate capacitance values of the DG and SG square-shaped extended TFET as a function of overdrive voltage (V_{OV}). Due to the formation of inversion layer of a TFET from the drain side toward the source side with increasing of V_{OV} , the regnant component in the capacitance between the gate and the inversion layer is gate-drain capacitance [32]. Increase in the V_{OV} causes gate-drain capacitance extremely increases which is proportional to gate length, as can be confirmed in Fig. 3(a). The gate-drain and gate-source capacitance values of DG square-shaped extended TFET are larger than SG square-shaped extended TFET which should be mainly due to the much larger coupling between the gate and the source. Due to the extension of the inversion layer from the drain side toward the source side and fewer coupling between the gate and the source, the gate-source capacitance monotonically decreases, as shown in Fig. 3(b).

Fig. 4 shows the transconductance (g_m) of DG and SG square-shaped extended TFETs as a function of overdrive voltage (V_{OV}). As can be seen, DG square-shaped extended TFETs have 350 times higher transconductance than SG structure at high V_{OV} . It should be mainly due to the higher

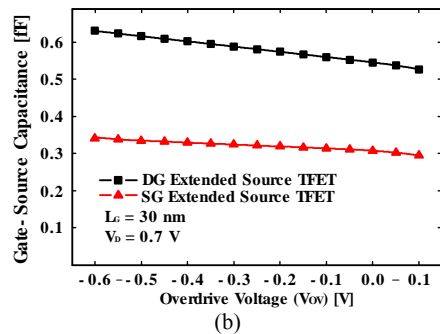
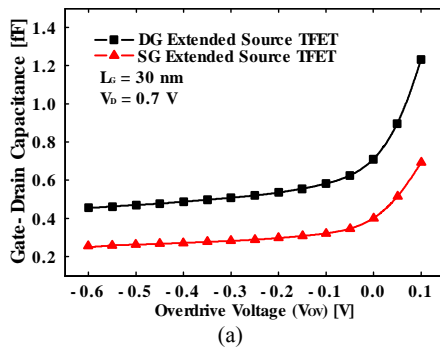


Fig. 3. Gate capacitance values of the DG and SG square-shaped extended source TFET as a function of V_{OV} . (a) gate-drain capacitance and (b) gate-source capacitance.

total field in between the source and channel that leads to an increase in the higher on-current and transconductance.

The RF figures of merit for extended source TFETs are analyzed in terms of cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}). The values of the cut-off and maximum oscillation frequencies have been extracted by high-frequency current gain and unilateral power gain using the TCAD-simulated Y-parameter data, respectively. Fig. 5 compares the f_T values of the DG and SG square-shaped extended TFETs as a function of V_{OV} . Generally, the cut-off frequency depends on the g_m , C_{gd} and C_{gs}

$$(f_T \propto \frac{g_m}{2\pi \times (C_{gd} + C_{gs})}).$$

Since C_{gg} (sum of the C_{gd} and C_{gs}) and g_m increase monotonically with the increase of V_{OV} as shown in Figs. 3 and 4, f_T of TFETs have the rising tendency as a function of V_{OV} . However the DG square-shaped extended TFETs have 350 times higher g_m than SG structures at high V_{OV} , f_T of DG square-shaped extended TFETs has improved only 150 times higher than that of SG structures. It is because the C_{gg} of DG square-shaped extended TFETs at high V_{OV} is about 2.3 times higher than that of SG structures.

Fig. 6 shows the f_{max} values of the DG and SG square-shaped extended TFETs obtained from unilateral power gains as a function of V_{OV} . DG square-shaped extended TFETs have higher f_{max} values than SG square-shaped extended TFETs because of lower channel resistance and higher f_T and g_m . The maximum f_{max} values of the DG and SG square-shaped extended TFETs were about 37.6, and 3.5 GHz at $V_{DS} = 0.7$ V, respectively. The results indicate

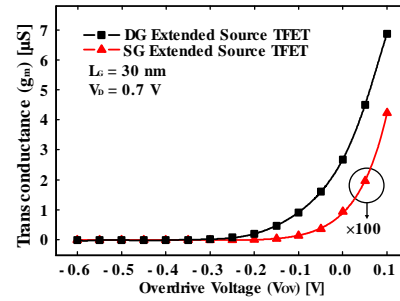


Fig. 4. Comparison of transconductance (g_m) between a DG and SG square-shaped extended source TFET as a function of overdrive voltage (V_{OV}).

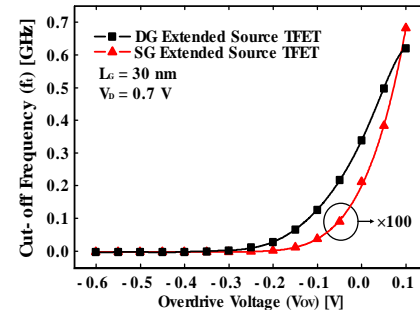


Fig. 5. Comparison of the f_T value between DG and SG square-shaped extended source TFET as a function of V_{OV} .

that DG square-shaped extended TFETs can have higher cut-off and maximum oscillation frequencies for high-frequency electronics applications.

The modeled Y -parameters by SPICE simulation were compared with the values obtained from TCAD simulation up to 250 GHz as shown in Fig. 7 in order to validate the parameter extraction. Table 1 summarize all the extracted parameters of the DG and SG square-shaped extended TFETs used in the verifications at $V_{GS} = 0.7$ V and $V_{DS} = 0.7$ V. As shown in Table 1 of manuscript, the values of approximations are much smaller than one even at 250 GHz ($\omega^2 R_g^2 (C_{gs} + C_{gd})^2 = 1.096 \times 10^{-3}$ and 3.353×10^{-3} ; $\omega^2 \tau^2 = 8.19 \times 10^{-3}$ and 6.44×10^{-3} for SG and DG square-shaped extended source TFET, respectively). This verifies the validity of using the assumption in simplifying (1)-(4) to (5)-(8) in this work up to extremely high frequency range even at 250 GHz. As seen, Y -parameters obtained from the NQS model equivalent circuit showed close agreement with the calculation results by the TCAD simulation. The root-mean-square errors of the model were calculated to be within 3.3% and 3.7% for the DG and SG square-shaped extended TFETs, respectively. These verification results strongly support that the proposed model is accurate and valid for extended source TFETs up to the extremely high frequency range.

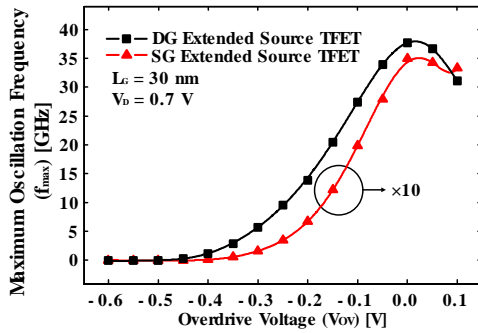
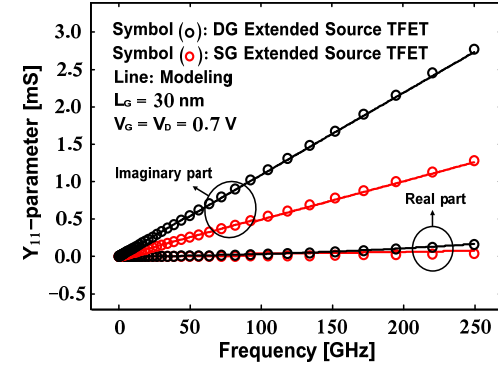


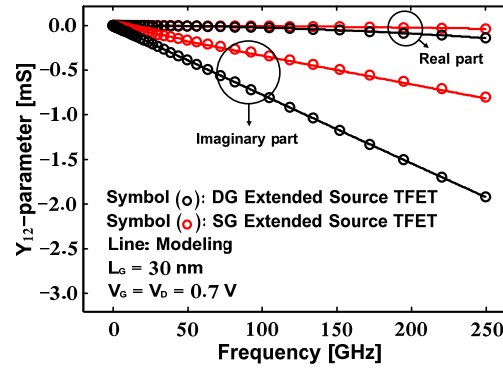
Fig. 6. Comparison of the f_{max} values between DG and SG square-shaped extended source TFET obtained from unilateral power gains as a function of V_{OV} .

Table 1. The summary of the extracted parameters ($V_{GS} = 0.7$ and $V_{DS} = 0.7$ V) for DG and SG square-shaped extended source TFET.

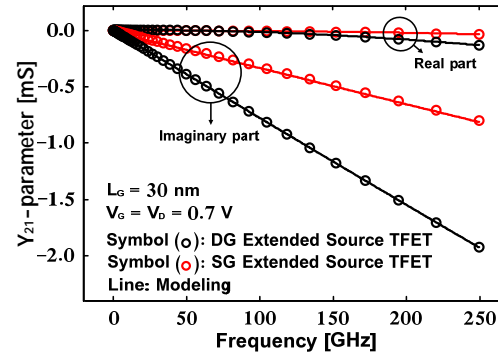
	SG square-shaped extended source TFET	DG square-shaped extended source TFET
C_{gs}	0.306 fF	0.528 fF
C_{gd}	0.513 fF	1.233 fF
C_{sd}	44.975 aF	14.649 aF
R_g	25.736 Ω	20.932 Ω
τ	0.362 ps	0.321 ps
g_m	19.618 nS	6.817 μ S
g_{ds}	34.214 pS	52.45 nS
$\omega^2 R_g^2 (C_{gs} + C_{gd})^2$	1.096×10^{-3}	3.353×10^{-3}
$\omega^2 \tau^2$	8.19×10^{-3}	6.44×10^{-3}



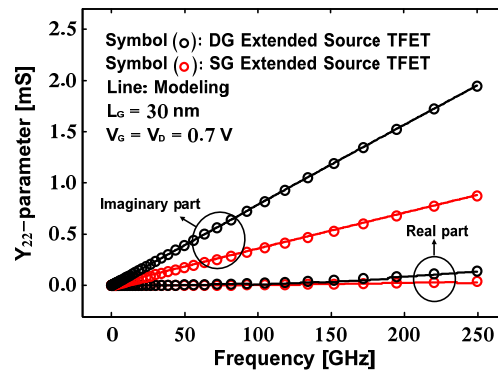
(a)



(b)



(c)



(d)

Fig. 7. Comparison of modeled (line) and values obtained from TCAD simulation (symbol) Y -parameters of DG and SG square-shaped extended source TFET at $V_{GS} = 0.7$ and $V_{DS} = 0.7$ V. (a) Y_{11} , (b) Y_{12} , (c) Y_{21} and (d) Y_{22} .

4. Conclusion

In this paper, we described RF performances of DG and SG square-shaped extended TFETs based on parameter extractions from the NQS model equivalent circuit in terms of the cut-off frequency, maximum oscillation frequency and small-signal parameters. DG square-shaped extended TFETs have higher RF performances because of the much higher transconductance than SG square-shaped extended TFETs. The results showed good agreement between the modeled Y-parameters and the extracted parameters for the high frequency range up to the cut-off frequency.

References

- [1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.
- [2] B. Rajamohanam, D. Mohata, A. Ali, and S. Datta, "Insight into the output characteristics of III-V tunneling field effect transistors," *J. Appl. Phys.*, vol. 102, pp. 092105-1–092105-5, 2013.
- [3] P. Guo, Y. Yang, Y. Cheng, G. Han, J. Pan, Ivana, Z. Zhang, H. Hu, Z. X. Shen, C. K. Chia, and Y. Yeo, "Tunneling field-effect transistor with Ge/In_{0.53}Ga_{0.47}As heterostructure as tunneling junction," *J. Appl. Phys.*, vol. 113, pp. 094502-1–094502-9, 2013.
- [4] S. Marjani and S. E. Hosseini, "Radio-frequency small-signal model of hetero-gate-dielectric p-n-p-n tunneling field-effect transistor including the charge conservation capacitance and substrate parameters," *J. Appl. Phys.*, vol. 118, pp. 095708-1–095708-8, 2015.
- [5] T. Yu, J. T. Teherani, D. A. Antoniadis and J. L. Hoyt, "In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5} quantum-well tunnel-FETs with tunable backward diode characteristics," *IEEE Electron. Device Lett.*, vol. 34, no. 12, pp. 1503–1505, 2013.
- [6] A. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. Redwing and T. Mayer, "Fabrication and characterization of axially doped silicon nanowire tunnel field-effect transistors," *Nano Lett.*, vol. 10, no. 10, pp. 4813–4818, 2010.
- [7] G. Dewey, B. Chu-Kung, J. Boardman, JM. Fastenau, J. Kavalieros, WK. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, HW. Then and R. Chau, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep subthreshold swing," in *Proc. of IEEE International Electron Device Meeting (IEDM)*, Washington, DC, USA, pp. 5–7, 2011.
- [8] J. S. Lee, J. H. Seo, S. Cho, J. Lee, S. Kang, J. Bae, E. Cho, and I. M. Kang, "Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors," *Current Appl. Phys.*, vol. 13, no. 6, pp. 1143–1149, 2013.
- [9] M. Luisier, G. Klimeck, "Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling," *J. Appl. Phys.*, vol. 107, no. 8, pp. 084507–084507-6, 2010.
- [10] S. Koswatta, S. Koester, and W. Haensch, "On the possibility of obtaining MOSFET-like performance and sub60mV/dec swing in 1-D broken-gap tunnel transistors," *IEEE Trans. Electron. Devices*, vol. 57, no. 12, pp. 3222–3230, 2010.
- [11] G. Han, P. Guo, Y. Yang, L. Fan, Y. S. Yee, C. Zhan, and Y.-C. Yeo, "Source engineering for tunnel field-effect transistor: elevated source with vertical silicon-germanium/germanium heterostructure," *Jpn. J. Appl. Phys.*, vol. 50, no. 4, pp. 04DJ07-1–04DJ07-4, 2011.
- [12] K. Ganapathi and S. Salahuddin, "Heterojunction vertical band-to-band tunneling transistors for steep subthreshold swing and high ON current," *IEEE Electron. Device Lett.*, vol. 32, no. 5, pp. 689–691, 2011.
- [13] Q. T. Zhao, J. M. Hartmann, and S. Mantl, "An improved Si tunnel field effect transistor with a buried strained Si1–3Ge source," *IEEE Electron. Device Lett.*, vol. 32, no. 11, pp. 1480–1482, 2011.
- [14] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science*, vol. 335, no. 6071, pp. 947–950, 2012.
- [15] S. Richter, C. Sandow, A. Nichau, S. Trelenkamp, M. Schmidt, R. Luptak, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Ω-Gated silicon and strained silicon nanowire array tunneling FETs," *IEEE Electron. Device Lett.*, vol. 33, no. 11, pp. 1535–1537, 2012.
- [16] K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.*, vol. 97, no. 3, pp. 033504-1–033504-3, 2010.
- [17] K-T. Lam, X. Cao, and J. Guo, "Device performance of heterojunction tunneling field-effect transistors based on transition metal dichalcogenide monolayer," *IEEE Electron. Device Lett.*, vol. 34, no. 10, pp. 1331–1333, 2013.
- [18] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-k gate dielectric," *IEEE Trans. Electron. Devices*, vol. 54, no. 7, pp. 1725–1733, 2007.
- [19] R. Jhaveri, V. Nagavarapu, and J. Woo, "Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor," *IEEE Trans. Electron. Devices*, vol. 58, no. 1, pp. 80–86, 2011.
- [20] H. Chang, B. Adams, P. Chien, J. Li, and J. C. S. Woo, "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Trans. Electron. Devices*, vol. 60, no. 1, pp. 92–96, 2013.
- [21] K. Kao, A. S. Verhulst, W. G. Vandenberghe, and K. De Meyer, "Counterdoped pocket thickness optimization of gate-on-source-only tunnel FETs," *IEEE Trans. Electron. Devices*, vol. 60, no. 1, pp. 6–12, 2013.
- [22] N. Damrongplasit, S. H. Kim, C. Shin, and T. K. Liu, "Impact of gate line-edge roughness (LER) versus random dopant fluctuations (RDF) on germanium-source tunnel FET performance," *IEEE Trans. Nanotechnol.*, vol. 12, no. 6, pp. 1061–1067, 2013.
- [23] G. Leung and C. Chui, "Stochastic variability in silicon double-gate lateral tunnel field-effect transistors," *IEEE Trans. Electron. Devices*, vol. 60, no. 1, pp. 84–91, 2013.
- [24] L. Lattanzio, N. Dagtekin, L. D. Michielis, and A. M. Ionescu, "On the static and dynamic behavior of the germanium electron-hole bilayer tunnel FET," *IEEE Trans. Electron. Devices*, vol. 59, no. 11, pp. 2932–2938, 2012.

- [25] Y. Yang, P. Guo, G. Han, K. L. Low, C. Zhan, and Y.-C. Yeo, "Simulation of tunneling field-effect transistors with extended source structures," *J. Appl. Phys.*, vol. 111, pp. 114514-1–114514-8, 2012.
- [26] Kanungo, H. Rahaman, P. S. Gupta, and P. S. Dasgupta, "Extended source ultra-thin body double-gated tunnel FET," in *Proc. of 5th International Conference on Computers and Devices for Communication (CODEC)*, Kolkata, India, pp. 1–4, 2012.
- [27] ATLAS Device Simulation Software, Silvaco Int., Santa Clara, CA, USA, 2012.
- [28] W. Hansch, T. Vogelsang, R. Kirchner, and M. Orlowski, "Carrier transport near the Si/SiO₂ interface of a MOSFET," *Solid State Electron.*, vol. 32, no. 10, pp. 839–849, 1989.
- [29] A. Schenk, "A model for the field and temperature dependence of SRH lifetimes in silicon," *Solid State Electron.*, vol. 35, no. 11, pp. 1585–1596, 1992.
- [30] B. Ghosh and M. W. Akram, "Junctionless tunnel field effect transistor," *IEEE Electron. Dev. Lett.*, vol. 34, no. 5, pp. 584–586, 2013.
- [31] I. Kwon, M. Je, K. Lee, and H. Shin, "A simple and analytical parameter-extraction method of a microwave MOSFET," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 6, pp. 1503–1509, 2002.
- [32] S. Cho, J. S. Lee, K. R. Kim, B.-G. Park, J. S. Harris, Jr., and I. M. Kang, "Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors," *IEEE Trans. Electron. Devices*, vol. 58, no. 12, pp. 4164–4171, 2011.



Saeid Marjani received the B.S. and M.S. degrees in electrical engineering from Arak Branch, Islamic Azad University, Arak, Iran, and the Ph.D. degree in electrical engineering from Ferdowsi University of Mashhad, Mashhad, Iran. His research interests include the design, modeling, fabrication, and characterization of nanoscale CMOS, tunneling FETs, optoelectronics, and photonic devices and analog integrated systems.



Seyed Ebrahim Hosseini received the B.Sc. degree in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, the M.Sc. degree from Tarbiat Modares University, Tehran, Iran, and the Ph.D. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2001. He is currently an Associate Professor of Electronics Engineering with the Ferdowsi University of Mashhad, Mashhad, Iran.