Journal of Electrical Systems and Signals, Vol. 1, No. 2,. 2013

A Low-noise Low-power MOSFET only Electrocardiogram Amplifier

Maryam Ghamati and Mohammad Maymandi-Nejad

Abstract: Electrocardiogram (ECG) signal is widely used in the diagnosis of heart diseases. Since the amplitude of this signal is very low, a high-gain low-noise amplifier with a high common mode rejection ratio (CMRR) is needed. In portable applications a battery provides the required power for the ECG device. Hence, ECG amplifiers should have low area and power consumption. In this paper, an instrumentation amplifier for ECG application is proposed in which MOSCAPs are used to reduce the circuit area. MOSCAPs are inherently nonlinear and a technique is presented to reduce the impact of this non-linearity. In ECG systems, a driven right-leg circuit is used to increase the CMRR of the amplifier. In this paper a class AB buffer is employed to implement this circuit. The simulation results show that the gain of the proposed amplifier is 46.18 dB and its input referred noise is 7.8 μV_{rms} over the frequency range of 0.3 Hz to 150 Hz. The total power consumption of the designed amplifier is 72 nW. The amplifier CMRR is 96 dB and its total harmonic distortion (THD) is 0,68% (at 60 Hz).

Keywords: Electrocardiogram(ECG), instrumentation amplifier, driven right-leg circuit, CMRR, MOSCAP.

1. Introduction

With ever increasing demand for portable biomedical instruments, the power consumption and area of these equipments should be decreased as much as possible. One of the widely used portable biomedical systems is the electrocardiogram (ECG) recording device. One of the main building blocks of this system is the ECG amplifier. The amplitude of the ECG signal is less than 5 mV and its frequency is between 0.5 to 200 Hz. Since this signal is very weak, in the first stage it should be amplified with a very low noise amplifier [1].

An ECG amplifier should be able to reject noise, offset and common mode voltage. Since the ECG signal contains low frequency components, the flicker noise has a major impact on the performance of the amplifier. Moreover, the ECG signal is taken from biopotential electrodes and passes through the electrode-skin interface, hence, a very large offset (>10 mV) exists at the input of the amplifier [1].

Manuscript received August 26, 2013; accepted October 27, 2013.
The authers are with the Departmant of Electrical Engineering, Ferdowsi University of Mashhad, Iran.
The corresponding author's email is: maryam.ghamati@gmail.com.

Therefore for the ECG signal to be amplified properly, the amplifier should omit this offset voltage; otherwise the amplifier may be saturated. Another unwanted signal is the common mode voltage that has the largest amplitude in 50/60 Hz frequency (coming from the power lines). Since the amplitude of this signal is much higher than that of the ECG signal, the amplifier should have a very high common mode rejection ratio (CMRR) to reduce the negative impact of this signal. However, ECG amplifiers with very high CMRR are power hungry and hence they are not suitable for portable applications. One solution is the utilization of driven-right-leg circuit. This circuit helps to reject the common mode voltage. Using the driven-right-leg circuit, amplifiers with moderate CMRR can be used and therefore, the overall power consumption of the system can be decreased. In portable applications, the right leg electrode is placed on the chest [2].

Different structures have been proposed for implementing ECG amplifier. These structures generally can be categorized into conventional and chopper amplifiers. Chopper amplifiers are able to reduce $1/f$ and DC noises considerably. However, since these structures are wide band, their power dissipation is high [1, 3]. Current mode amplifiers are one of the conventional biomedical structures. These amplifiers use folded cascode technique and are very power hungry. Gm-C filters are employed to omit offset and noise signals, but the drawback of these circuits is their high power dissipation [4, 5].

Typically, the gain of conventional instrumentation amplifiers is provided by resistor dividers. These amplifiers are noisy and power consuming. Also, due to the poor matching of resistors, the CMRR of this circuit is inherently low. However, the input impedance of this structure is high and the common mode voltage is generated without any peripheral circuit [2, 4]. Even if the resistors of these amplifiers are implemented using transistors, its power consumption is still a problem [6]. In [2] resistors are replaced with capacitors and the behavior of the circuit is improved with regard to noise and power [2]. However, since the low cut-off frequency of the ECG amplifier should be less than 0.5 Hz, the capacitors have become very large. Therefore this structure is not area efficient and suitable for portable applications.

In this paper a new ECG amplifier is presented in which capacitors are replaced with MOSCAPs. Using this technique the occupied area of the circuit on silicon is reduced. MOSCAPs are inherently nonlinear and techniques have so far been presented to solve this problem. In the proposed circuit input transistors are biased in sub-threshold region to save power. Also, a class AB buffer

is employed in the driven-right-leg circuit to enhance the CMRR.

The rest of this paper is organized as follow. In section 2 the structure of the proposed amplifier and the driven-right-leg circuit are explained. The linearization technique and analysis of its behavior are provided in section 3. Section 4 includes simulation results. The paper concludes in section 5.

2. The Amplifier Structure

The biomedical amplifier is usually a two stage circuit. In low voltage applications, it is not possible to cascode transistors and hence the gain of a single stage is not high. Instead, the stages are cascaded to achieve high gain. The first stage of an instrumentation amplifier (IA) is a low-noise low-gain circuit that generates the common mode voltage (V_{cm}). The second stage is a high gain and variable gain differential amplifier. The amplifier that is designed in this work is based on the amplifier architecture shown in Fig. 1 [2]. As can be seen in this figure, the resistors used in conventional IAs are replaced with capacitors. Using proper values for capacitors the low cut off frequency can be set to the desired value. Also, the DC common mode and offset voltage of the first stage is removed by the coupling capacitors C_5 and C_6. The disadvantage of using capacitors is the large area of the overall amplifier. One technique that can be used to tackle this problem is using MOSCAPs instead of the MIM capacitors since the area of MOSCAPs is ¼ of that of the MIM capacitors in the 0.18µm CMOS technology.

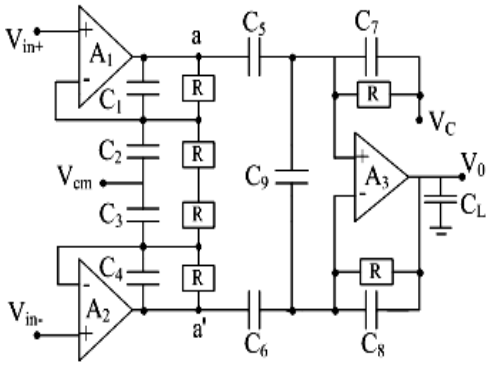

Fig. 1. The circuit diagram of the instrumentation amplifier [2].

A. The Operational Transconductance Amplifier

As shown in Fig. 1 the IA includes three operational transconductance amplifiers (OTA). The OTA structure employed in this design is illustrated in Fig. 2. The input transistors of the circuit are PMOS. Flicker noise of PMOS transistors are one to two orders of magnitude smaller than their NMOS transistors [2]. For further reduction of the input referred noise of the amplifier, the size of the input transistors is selected large and to reduce the power consumption they are biased in sub-threshold region [2]. Since the noise of the first stage is the most dominant part of the input referred noise of the circuit, the biggest part of the amplifier power budget is considered for this stage.

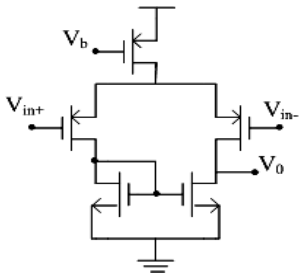

Fig. 2. The OTA structure.

B. Driven-Right-Leg Circuit

The driven-right-leg circuitcan help reject the common mode voltage using common mode feedback technique and hence prevents the amplifier from saturating due to the large amplitude of the common mode signal. The driven-right-leg circuit is one of the main blocks in ECG recording devices. The block diagram of this circuit is shown in Fig. 3. The circuit consists of an amplifier (OTA) and a buffer.

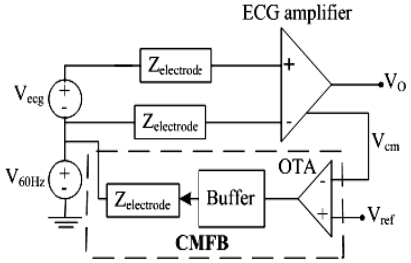

Fig. 3. Driven-right-leg circuit.

In order to reduce the power consumption of the driven-right-leg circuit, we have used a class AB buffer in the proposed architecture, so the CMRR does not reduce in low power consumption. The circuit diagram of this buffer is depicted in Fig. 4. Class AB amplifiers consume less power compared to class A amplifiers. The reason of using this structure for the buffer is its low distortion [7].

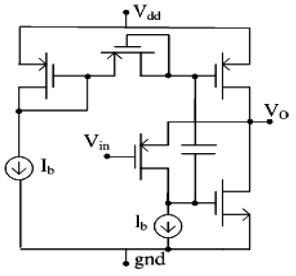

Fig. 4. The structure of the class AB buffer [7].

In our design the power budget of each stage is divided as shown in Table 1. Since the first stage of the instrumantion amplifier has a small gain and also has the most proportion in the total noise of the amplifier, the biggest part of power consumption (more than 50%) is

dedicated to this stage. The second stage of the amplifier is an OTA and has a bigger gain compared to the first stage. Therfore its impact on the input referred noise of amplifier is less than the first stage. Hence, power cosumption of the second satge can be less than first one (about 50%). Since the driven right-leg circuit using a Class-AB and its OTA are not required to have a high gain and large bandwidth, the least proportion of the total power dissipation of the amplifier is dedicated to this circuit.

Table 1. The Considered Power for each Stage of the Amplifier.

Stages	Power	Power percentage for each stage
First stage	42nW	58.3%
Second stage	22nW	30.5%
The OTA used in the driven-right-leg circuit	1nW	1.38%
Driven-right-leg buffer	5nW	6.9%

3. Circuit Linearization

A. MOSCAP and Semi-Resistor Linearization

Since the designed amplifier should operate as a filter, its low cut-off frequency should be less than 0.5 Hz. For achieving this, capacitors should be enlarged. It means that the occupied area of capacitors and consequently circuit area is increased. In order to prevent this problem MOSCAPs instead of MIM capacitors are used.

We have replaced the MIM capacitors of the ECG amplifier with MOSCAPs in order to save the area. MOSCAPs are inherently non-linear and using them in a circuit can result in output voltage distortion. Fig. 5 shows the variation of the capacitance of a MOSCAP versus the voltage difference between its terminals [8].

Fig. 5 illustrates different operating regions of a MOSCAP including accumulation, depletion and inversion regions. The variation of the capacitor size is not large in the accumulation and inversion regions, but it is very nonlinear in the depletion region. In order to place a MOSCAP in the accumulation and inversion regions, the voltage difference across its terminals should be high [8, 9]. There are three ways for linearization of MOSCAPs. We can put these devices in series or in parallel as illustrated (Fig. 6-b and c). Alternatively, we can increase the gate to bulk voltage of the MOSCAP to place it in inversion region [9].

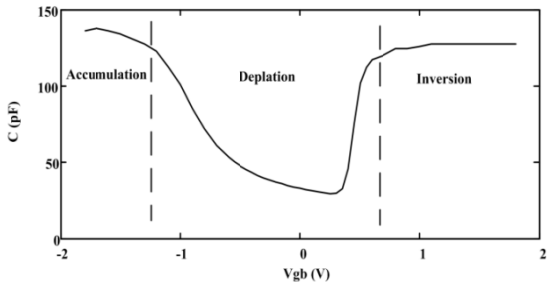

Fig. 5. The capacitance of the MOSCAP versus its gate-body voltage in different region [8].

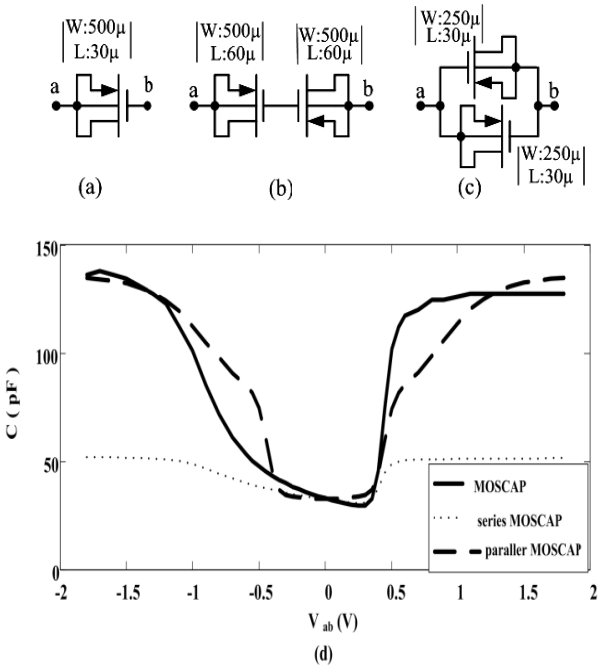

Fig. 6. a) Circuit diagram of a MOSCAP, b) MOSCAPs in series, c) MOSCAPs in parallel, d) Variation of the capacitance of a MOSCAPs versus the voltage difference between its terminals.

As shown in Fig. 6(d), series connection of MOSCAPs is linear for voltages more than about 0.5V. However, it leads to small values of capacitance and the area should be increased by a factor of approximately 4 to reach the same capacitance obtained by a simple MOSCAP. Therefore, using series combination is not a suitable solution for the linearization of MOSCAPs in our design. Parallel connection of MOSCAPs is linear when voltage difference between its terminals is 0 V. The occupied area of this structure is the same as an individual MOSCAP.

Another element of the ECG amplifier that takes a large area is the resistors (R blocks in Fig. 1). It is possible to use MOSFETs as resistors to save area. Two possible structures for implementing these resistors are shown in Fig. 7. The didoe-connected structure shown in Fig. 7-b is more linear than the gete-source short-circuited strcture shown in Fig. 7-a [10]. If gate-source voltage in the diode-connected structure is about zero, we can access a ristance as large as 10^{12} Ω [11]. We have used the diode connected configuration of Fig. 7-b in our design.

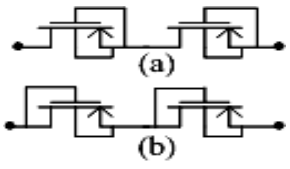

Fig. 7. Semi-resistor structures [10].

B. THD Analysis

In this sub-section, first the effect of capacitors nonlinearities on the amplifier output is analyzed. In the next step according to the result of this analysis, the structures of MOSCAPs are selected.

In order to analyze the linearity of our circuit and investigation of the effect of each MOSCAP on the circuit behavior, we consider a simple form of the ECG amplifier as illustrated in Fig. 8. Assuming the input voltage is sinusoidal; i.e. $v_i = A\cos(\omega t)$. In order to model the nonlinearity of the capacitors, we assume a first order model; i.e.

$$C_i = c_i(1+\alpha_i V_i) \quad (1)$$

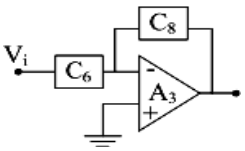

Fig. 8. The simplified circuit of the second stage for analyzing the THD.

Using Equation (1) for the capacitors we have calculated the THD at the output of the second stage amplifier. This leads to

$$THD_2 \approx (\alpha_6 + \alpha_8 G)\frac{A}{2}, \qquad G = \frac{c_6}{c_8}. \quad (2)$$

According to (2), the nonlinearity coefficient of C_8 (α_8) is multiplied by the second stage voltage gain (G). Hence, this capacitor has an important role in the THD.

If we desire to improve the THD and the circuit area is not very important, we can implement x percentage of C_8 using MOSCAP and the rest of it using MIM capacitor as it can be seen in Equation (3). Assuming x percentage of C_8 is MOSCAP, the THD can be obtained to be:

$$C_8 = xc_8(1+x\alpha_8 V_8) + (1-x)c_8 \quad (3)$$

$$THD_2' \approx (\alpha_6 + x^2\alpha_8 G)\frac{A}{2}, \qquad G = \frac{c_6}{c_8}. \quad (4)$$

Regarding (4), if we realize 70% C_8 with MOSCAP, THD is halved compared to the case when all C_8 is completely implemented by MOSCAPs. However, the area of this capacitor becomes 1.9 times larger. Therefore, area in our design is important, we implement C_8 using parallel MOSCAP.

Since C_1 to C_4 are in the first stage of the amplifier, if their nonlinearity is modeled in (1), the THD for the first stage of Fig. 9 can be calculated by (5).

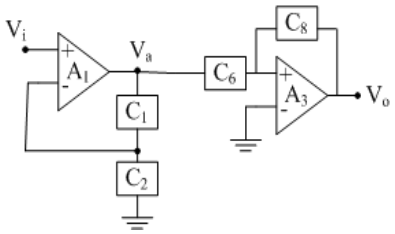

Fig. 9. The simplified circuit for analyzing the THD.

$$THD_1 \approx \frac{\frac{A.c_2}{2c_1}(\alpha_2 - \frac{c_2.\alpha_1}{c_1})}{1+\frac{c_2}{c_1}}. \quad (5)$$

According to (5), nonlinearity of first stage capacitors does not affect the output nonlinearity, since the values of C_1 and C_2 are equal.

C. Choosing MOSCAPs Structures in Instrumentation Amplifier

As mentioned before, MOSCAPs are very nonlinear in different operating regions and some approaches for solving this problem have been investigated in previous sections. According to (2), C_7 and C_8 that are shown in the instrumentation amplifier of Fig. 1 have the most impact on the output voltage nonlinearity. This is because their nonlinearity coefficients are multiplied by the voltage gain of the second stage. With respect to the resistant feedback path between the input and output of the second stage OTA (Fig. 1), the voltage difference across C_7 and C_8 are zero. Hence for reducing the occupied area by these capacitors, we use two MOSCAPs in parallel. In this technique, MOSCAPs is very linear when the voltage difference across its terminals is zero and its area can be reduced to ¼ of MIM to achieve the same capacitance.

Since the first stage is designed for achieving low noise and low common mode voltage and also it has a low voltage gain, C_1 and C_2 are selected equal. Therefore, the voltage gain of the first stage will become 2. According to (5), if C_1 and C_2 are equal, the THD becomes zero and hence the nonlinearity of these capacitors doesnot have any effect on the circuit linearity.

Referring back to the circuit structure, the voltage of the 'a' node is half of the supply voltagefor proper operation of OTA and V_{cm} is about zero. Hence, the voltage differences across C_1 to C_4 are not zero and we cannot usetwo MOSCAPs in parallel. Since these capacitors don't have any effect on the circuit THD, we can employ a single MOSCAP. Simulation results confirm the functionality of the described design.

In order to design the circuit with a low cut-off frequency less than 0.5 Hz, C_5 and C_6 are selected merely equal to 45 pF. This results in large capacitors, even if we use MOSCAPs in depletion region. Therefore, MOSCAPs in inversion and accumulation regions with low voltage differences are employed and its area can be reduced to $\frac{1}{16}$ of MIM to achieve the same capacitance.

For these capacitors we have used single transistor MOSCAPs but we have biased them in the inversion region to obtain linear operation and maximum capacitance. In the amplifier of Fig. 1, the dc voltage drop across C_5 and C_6 is close to 0 V which is not desirable. If we want to put a MOSCAP in inversion region, a voltage drop of minimum 0.6 V is needed (Fig. 5). In our design we have used a level shifter at the output of the first stage (nodes 'a' and 'a'' in the Fig. 1 to provide this voltage across C_5 and C_6. The structure of the level shifter is the same as the buffer in

Fig. 4. Using voltage level shifters, the voltage at 'a' and 'a'' nodes are increased to more than 0.9 V. However if these voltages are increased more, the output voltage nonlinearity is increased. Hence, the voltage difference across C_5 and C_6 will be more than 0.5 V.

Note that the voltage variation across C_5 and C_6 is very small and the non-linearity of these capacitors on the THD of the overall amplifier is negligible. By this voltage shift we have able to reduce the area of the C_5 and C_6 MOSCAPs by approximately 70%.

Table 2 shows the technique used to implement each of the capacitors of the ECG amplifier.

Table 2. The technique used for implementing the capacitor.

Capacitors	Way of implementation
C_1-C_4	Individual MOSCAP
C_5-C_6	Biased MOSCAPs with high voltage
C_7-C_9	MOSCAPParallel

4. Simulation Results

The proposed amplifier is simulated in 180 nm CMOS technology using TSMC model. The voltage supply is set to 1 V. The characteristic of the amplifier is reported in Table 3. The frequency response of the amplifier is depicted in Fig. 10(a). Fig. 10(b) illustrates the amplifier output noise versus frequency.

The CMRR variation of the class A and class AB circuits versus frequency are depicted in Fig. 11. In this simulation it is assumed that both circuits have the same power dissipation. Class AB has very better CMRR (30 dB higher than class A at 60 Hz). The obtained THD in different frequencies along with common mode voltage (V_c) are reported in Table 4.

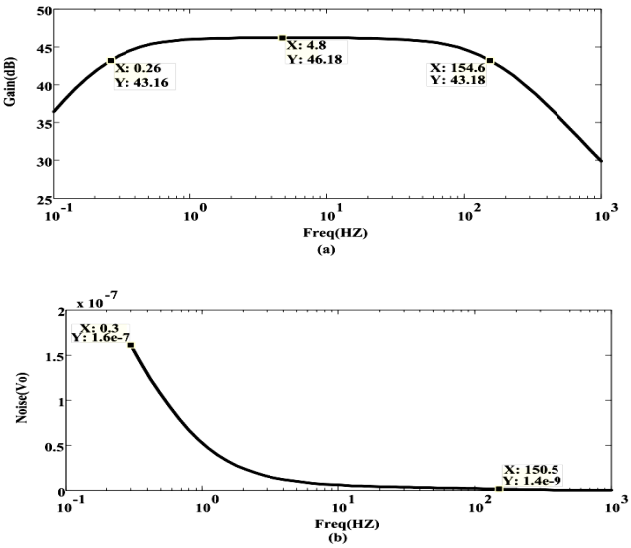

Fig. 10. (a) The frequency response of the amplifier. (b) Output noise.

Table 3. Performance parameters of the designed amplifier.

Gain	Bandwidth	Total power dissipation	Noise
46.18 dB	0.3-150 Hz	72 nW	7.8 μV_{rms}

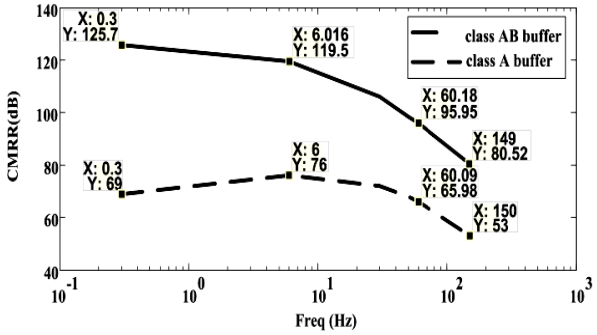

Fig. 11. The class A and AB CMRR in different frequencies.

Table 4. The THD in different frequencies.

[V_{in}=2mV , f_{in}= 30Hz]	THD=1.16%
[V_{in}=2mV , f_{in}= 50Hz]	THD=0.83%
[V_{in}=2mV , f_{in}= 60Hz]	THD=0.68%
[V_{in}=2mV , f_{in}= 100Hz]	THD=0.31%
[V_{in}=2mV , f_{in}= 100Hz] [V_c=2mV , f_{in}= 50Hz]	THD=0.94%

To achieve a variable gain we can implement C_7 and C_8 using tunable capacitors (Fig. 12). All of the capacitors of Fig. 12 are implemented by parallel MOSCAPs. The frequency response of the implemented amplifier using this technique for changing the gain is shown in Fig. 13.

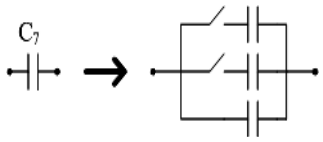

Fig. 12. The diagram of the variable capacitor.

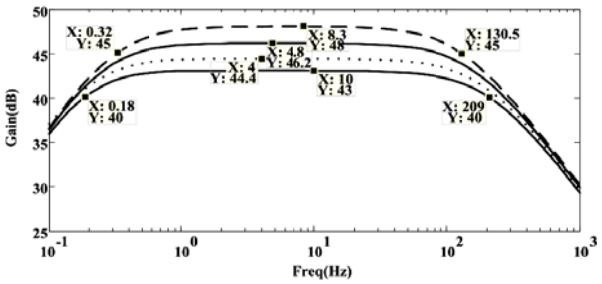

Fig.13. The frequency response of the designed amplifier with variable-gain.

The characteristic of the designed amplifier is compared with previous works in Table 5. As shown in this table the power consumption of the circuit is reduced much while other parameters are not changed considerably.

Table 5. Comparison of the proposed circuit with prior works.

	Power (W)	Gain (dB)	Noise (μV_{rms})	BW (Hz)	CMRR (dB)	Technology
[1]	2.1 µ	20	6.7	0.5-100	110	65nm
[2]	2.8 µ	45.3	8.1	290	90 at 60 Hz	0.5µm
[3]	46.8 µ	46	0.68	0.1-150	107	0.18µm
[4]	138 µ	45	0.27	0.2-200	127	0.18µm
[5]	110 µ	38	1.6	0.1-150	80	0.18µm
[11]	233 n	48-59	42	7-280	>80	0.13µm
This work	72 n	43-48	7.8	0.3-150	96 at 60 Hz	0.18µm

5. Conclusion

In this paper we use instrumentation structure for ECG application. In the proposed architecture we employ MOSCAPs instead of capacitors to reduce the area of the amplifier. As a result of replacing the MIM capacitors with MOSCAPs, the total area of the ECG amplifier is reduced by a factor of 10. We also use techniques for linearization of MOSCAPs and the amplifier provides output voltage swing of 0.4 V_{P-P} with total harmonic distortion of -50.17 dB at 100 Hz. The total power consumption of the amplifier and driven-right-leg circuit is reduced to 72 nW while the important parameters of the amplifier are kept comparable to similar works. This result is achieved using class AB buffer and biasing transistors of the OTA in the sub-threshold region. The input referred noise of the amplifier is equal to 7.8 μV_{rms} and the amplifier CMRR is 96 dB at frequency 60 Hz.

References

[1] Q. Fan, F. Sebastiano, and K. Makinwa, "A 2.1 µW area-efficient capacitively-coupled chopper instrumentation amplifier for ECG applications in 65 nm CMOS," *IEEE Asian Solid-State Circuits Conference (A-SSCC),* pp. 1-4, Nov. 2010.

[2] L. Fay, V. Misra, and R. Sarpeshkar, "A micropower electrocardiogram amplifier," *IEEE Transaction Biomedical Circuit and System*, vol. 3, no. 5, pp. 312-320, Oct. 2009.

[3] X. Yang, Q.i Cheng, L. Lin, W. Huang, and C. Ling, "Design of low power low noise amplifier for portable electrocardiogram recording system applications," *IEEE International Conference Anti-Counterfeiting, Security and Identification (ASID),* pp. 89-92, June 2011.

[4] C. Nanda, J. Mukhopadhyay, D. Mandal, and S. Chakrabarti, "1 V CMOS instrumentation amplifier with high DC electrode offset cancellation for ECG acquisition systems," *IEEE Students' Technology Symposium (TechSym),* pp. 21-25, April 2010.

[5] C. Hsu, C. Huang, K.Siong, W. Hsiao, and C. Wang, "A high performance current-balancing instrumentation amplifier for ECG monitoring systems," *International SoC Design Conference (ISOCC),* pp. 83-86, Nov. 2009.

[6] M. Goswami and S. Khanna, "DC suppressed high gain active CMOS instrumentation amplifier for biomedical application," *International Conference on Emerging Trends in Electrical and Computer Technology (ICETECT),* pp. 747-751, March 2011.

[7] A.J. Lopez-Martin, J. Ramirez-Angulo, R.G. Carvajal and L. Acosta, "Power efficient class AB CMOS buffer," *Electronics Letters,* vol. 45, no. 2, Jan. 2009.

[8] M. Saberi and R. Lotfi, "Analysis of the linearity of pipelined ADC due to capacitor non-linearity," *IEEE International Conference on Electronics, Circuits and Systems (ICECS),* pp. 403-406, Dec. 2009.

[9] T. Tille, J. Sauerbrey, Manfred Mauthe, and D. Schmitt-Landsiedel, "Design of low-voltage MOSFET-only ΣΔ modulators in standard digital CMOS technology," *IEEE Transactions on Circuts and Systems,* vol. 51, no. 1, pp. 96-109, Jan. 2004.

[10] H. Liu, K. Tang, J. Wu and G. Wang, "A digitally trimmable low-noise low-power analog front-end for EEG signal acquisition," *IEEE-EMBS International Conference on Biomedical and Health Informatics,* pp. 208-211, Jan. 2012.

[11] J. Y. Um, J. Y. Sim, and H. J. Park, "A gate-leakage insensitive 0.7-V 233-nW ECG amplifier using non-feedback PMOS pseudo-resistors in 0.13-µm N-well CMOS" *Journal of Semiconductor Technology and Science,* vol. 10, no. 4, pp. 309-315, Dec. 2010.

Maryam Ghamati received the B.Sc. degree from Sadjad Institute of Higher Education, Mashhad, Iran, in 2009 and M.Sc. degree in electrical engineering from Ferdowsi University of Mashhad, Mashhad, Iran, in 2013. Her research interests are low-voltage, low-power biomedical circuits and systems.

Mohammad Maymandi-Nejad received the B.Sc. degree from Ferdowsi University of Mashhad, Mashhad, Iran, in 1990, the M.Sc. degree from Khajeh Nassir Tossi University of Technology, Tehran, Iran, in 1993, and the Ph.D. degree from the University of Waterloo, Waterloo, ON, Canada, in 2005, all in electronics engineering.

From 1994 to 2001, he was a Lecturer in the Department of Electrical Engineering, Ferdowsi University of Mashhad, where he was engaged in teaching and research and also conducted several industrial projects in the field of automation and computer interfacing. He is currently an Associate Professor in the same department. His current research interests include low-voltage, low-power analog and mixed mode ICs and their applications in biomedical circuits and systems.

Mohammad Maymandi-Nejad received the Strategic Microelectronics Council of Information Technology Academia Collaboration (ITAC) Industrial Collaboration Award in 2005 for his work on a wireless bioimplantable device for monitoring blood pressure of transgenic mice.